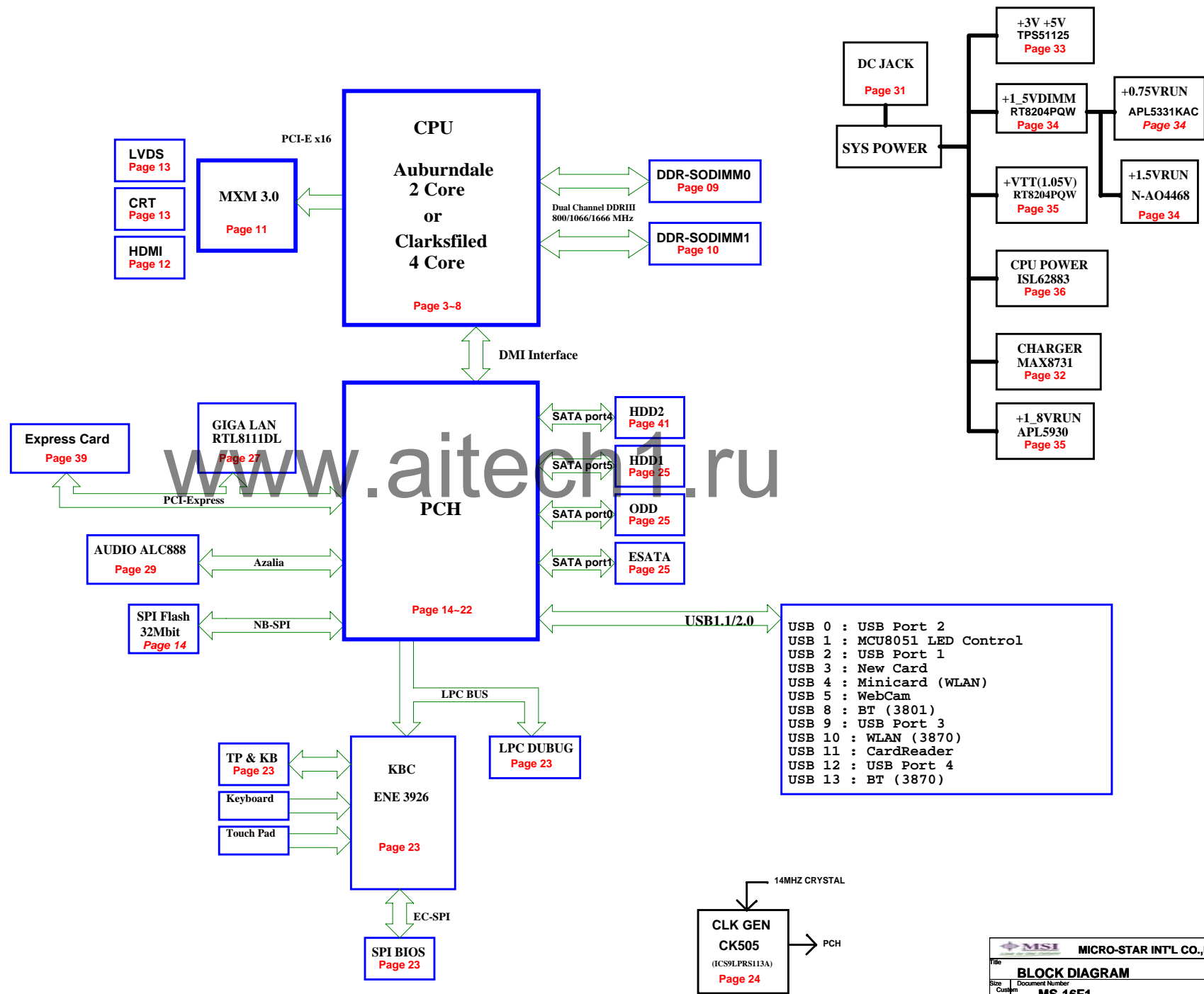


## Calpella Platform

- 01 : BLOCK DIAGRAM  
 02 : PLATFORM  
 03 : PROCESSOR-1 (HOST BUS)  
 04 : PROCESSOR-2 (DDR3)  
 05 : PROCESSOR-3 (POWER)  
 06 : PROCESSOR-4 (GRAPHICS POWER)  
 07 : PROCESSOR-5 (GND)  
 08 : PROCESSOR-6 (RESERVE)  
 09 : DDR3 SODIMM 0  
 10 : DDR3 SODIMM 1  
 11 : MXM3.0 Slot  
 12 : HDMI  
 13 : CRT/LVDS/CCD  
 14 : PCH-1 (HDA/JTAG/SATA)  
 15 : PCH-2 (PCI-E/SMBUS/CLK)  
 16 : PCH-3 (DMI/FDI/GPIO)  
 17 : PCH-4 (LVDS/DDI)  
 18 : PCH-5 (PCI/USB/NVRAM)  
 19 : PCH-6 (GPIO/NCTF/RSVD)  
 20 : PCH-7 (POWER)  
 21 : PCH-8 (POWER)  
 22 : PCH-9 (GND)  
 23 : KBC/EC/uP (KB3926)  
 24 : Clock Generator (ICS9LPRS113A)  
 25 : HDD2/ODD/ESATA/FAN/BT  
 26 : Card Reader (UB6250)  
 27 : GIGA LAN (RTL8111DL)  
 28 : WLAN/TP/BTB/USB  
 29 : AUDIO (ALC888)  
 30 : LED 8051  
 31 : M\_Battery select  
 32 : M\_Battery Charger  
 33 : M\_System Power  
 34 : M\_DIMM\_1.5VRUN  
 35 : M\_VTT\_1.8VRUN  
 36 : M\_CPU power  
 37 : Screw  
 38 : EMI  
 39 : 16F1A\_NewCard/HDD1  
 40 : 16F1B\_I/O/Audio Board  
 41 : 16F1C\_HDD2  
 42 : 16F1D\_CapSensor Board  
 43 : 16F1E\_Touch Pad L/R Key  
 44 : 16F1F\_CDLED\_RF  
 45 : 16F1G\_ABLED Front  
 46 : 16F1H\_ABLED\_L  
 47 : 16F1I\_ABLED\_R  
 48 : 16F1J\_CDLED\_L  
 49 : 16FK\_CDLED\_LF  
 50 : PowerDown Sequency  
 51 : PowerOn Sequency  
 52 : History



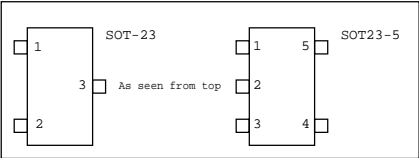
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions

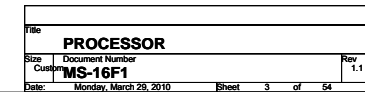
Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints

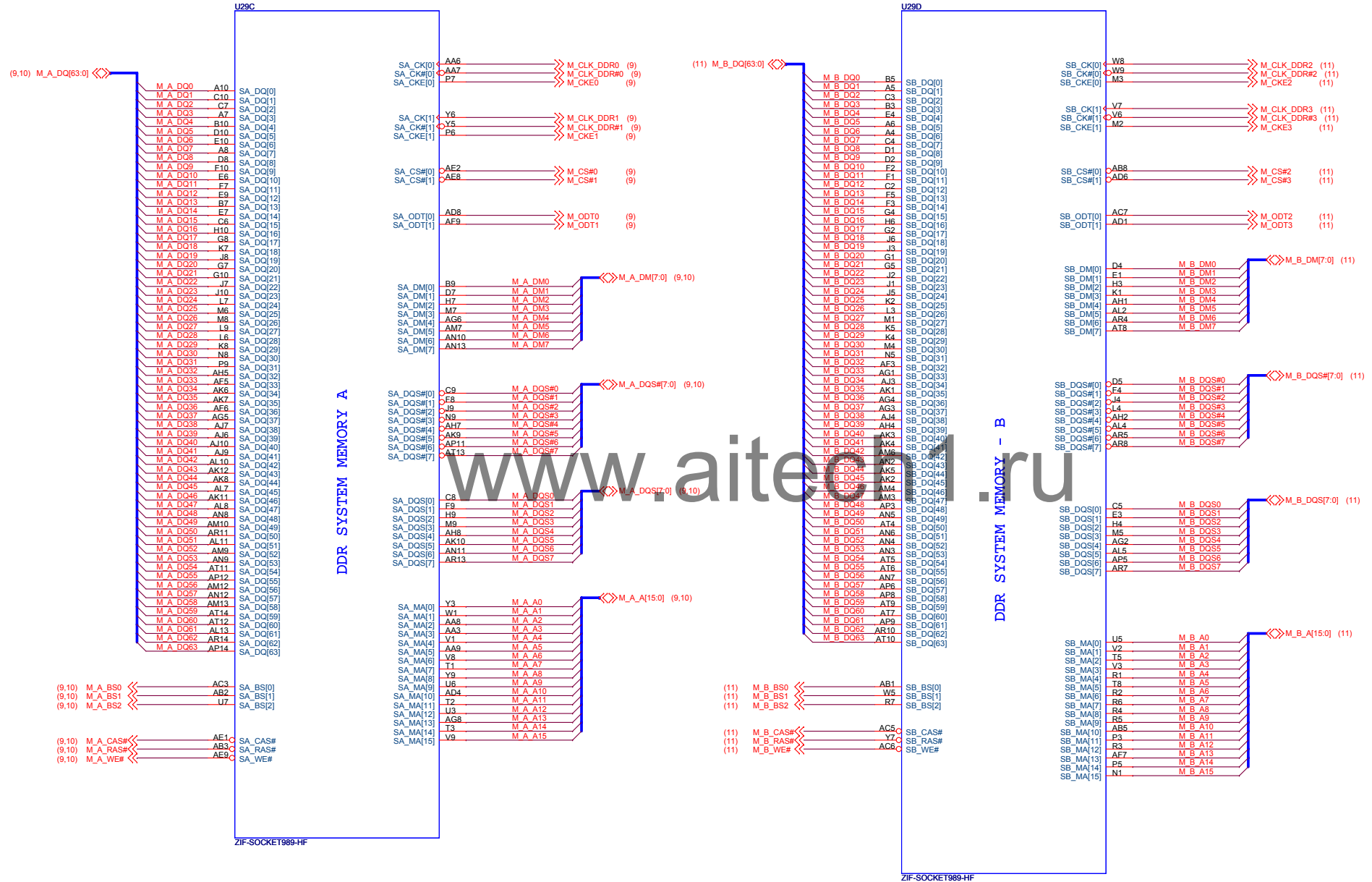


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Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

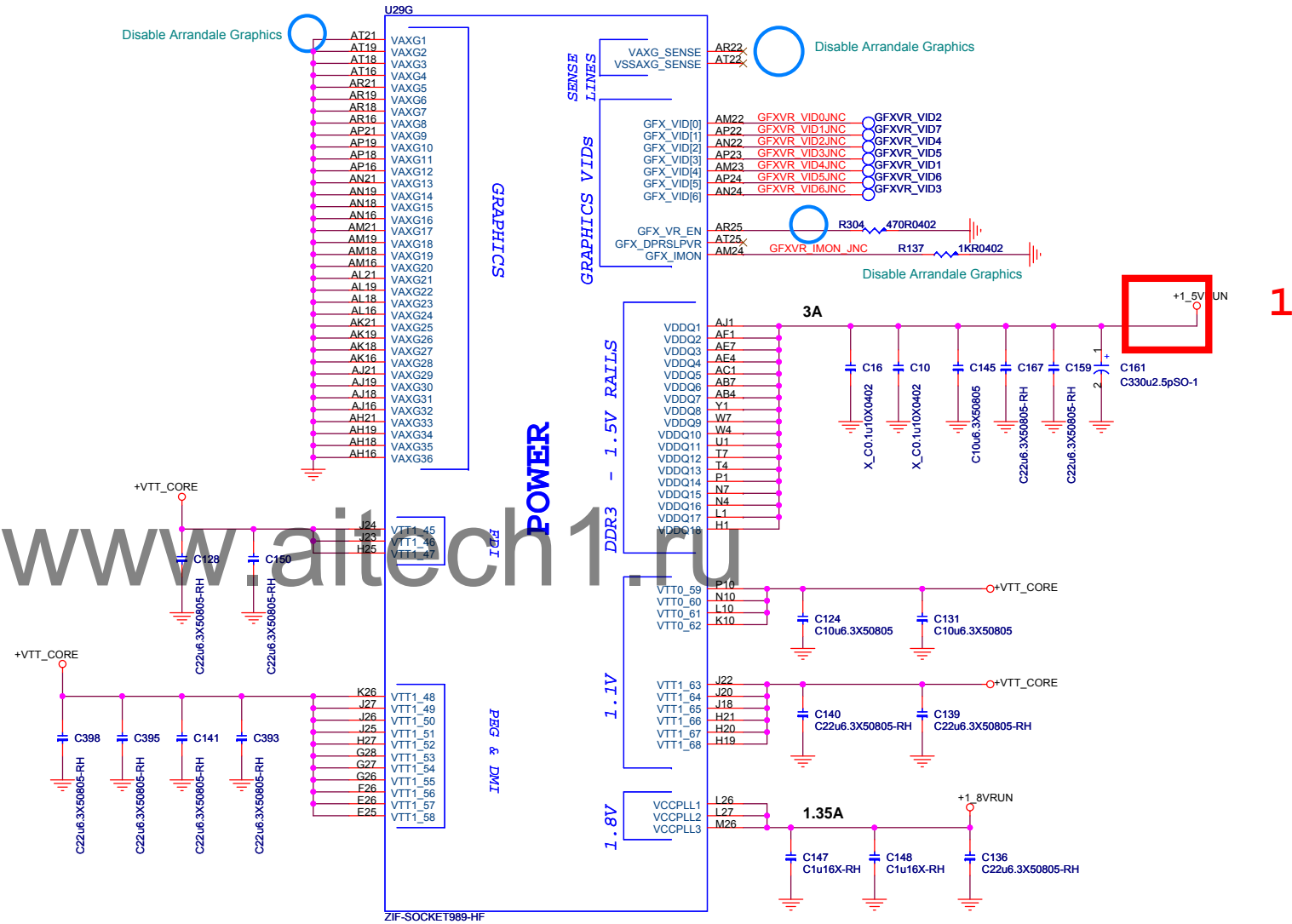


# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

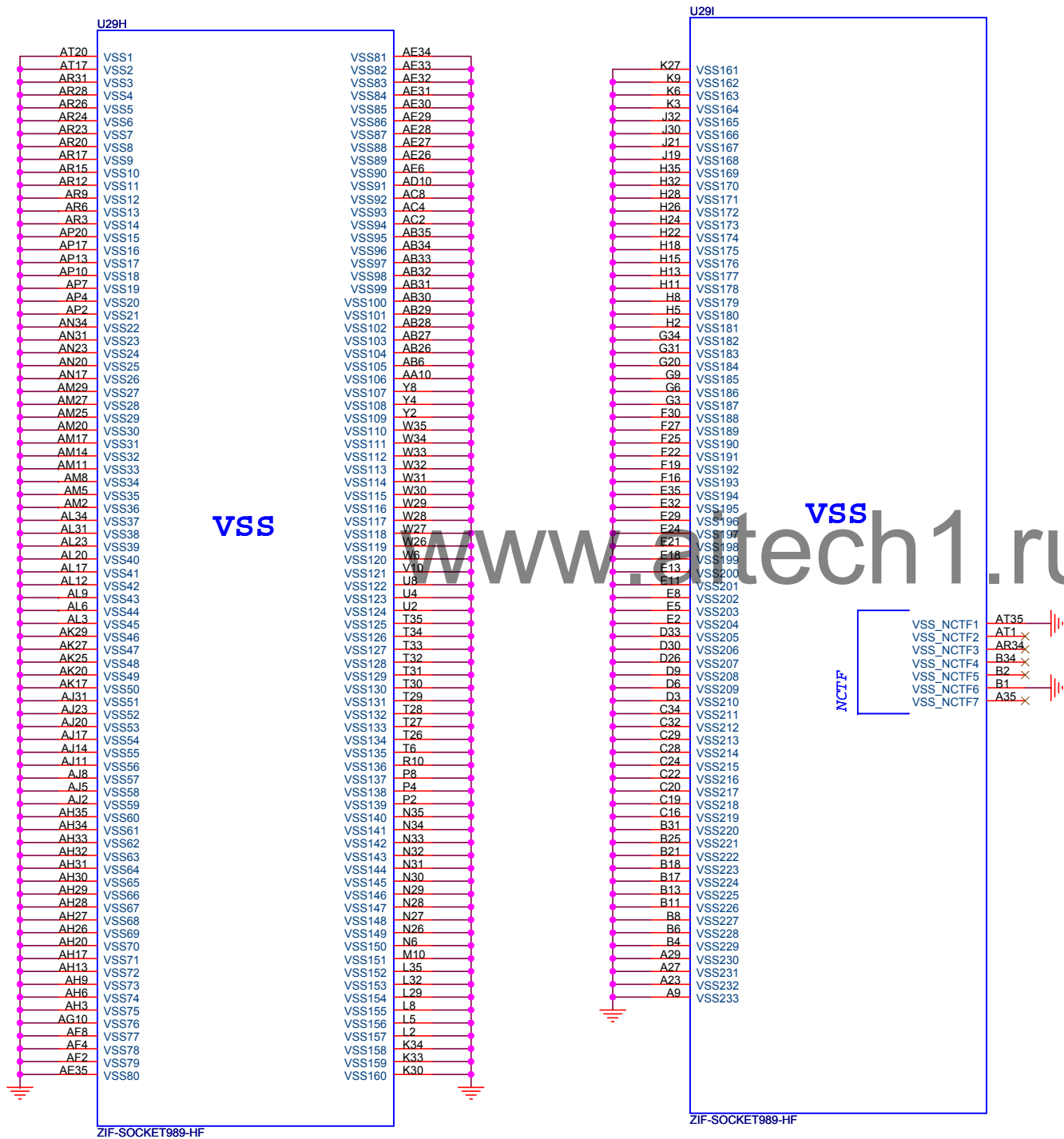




AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

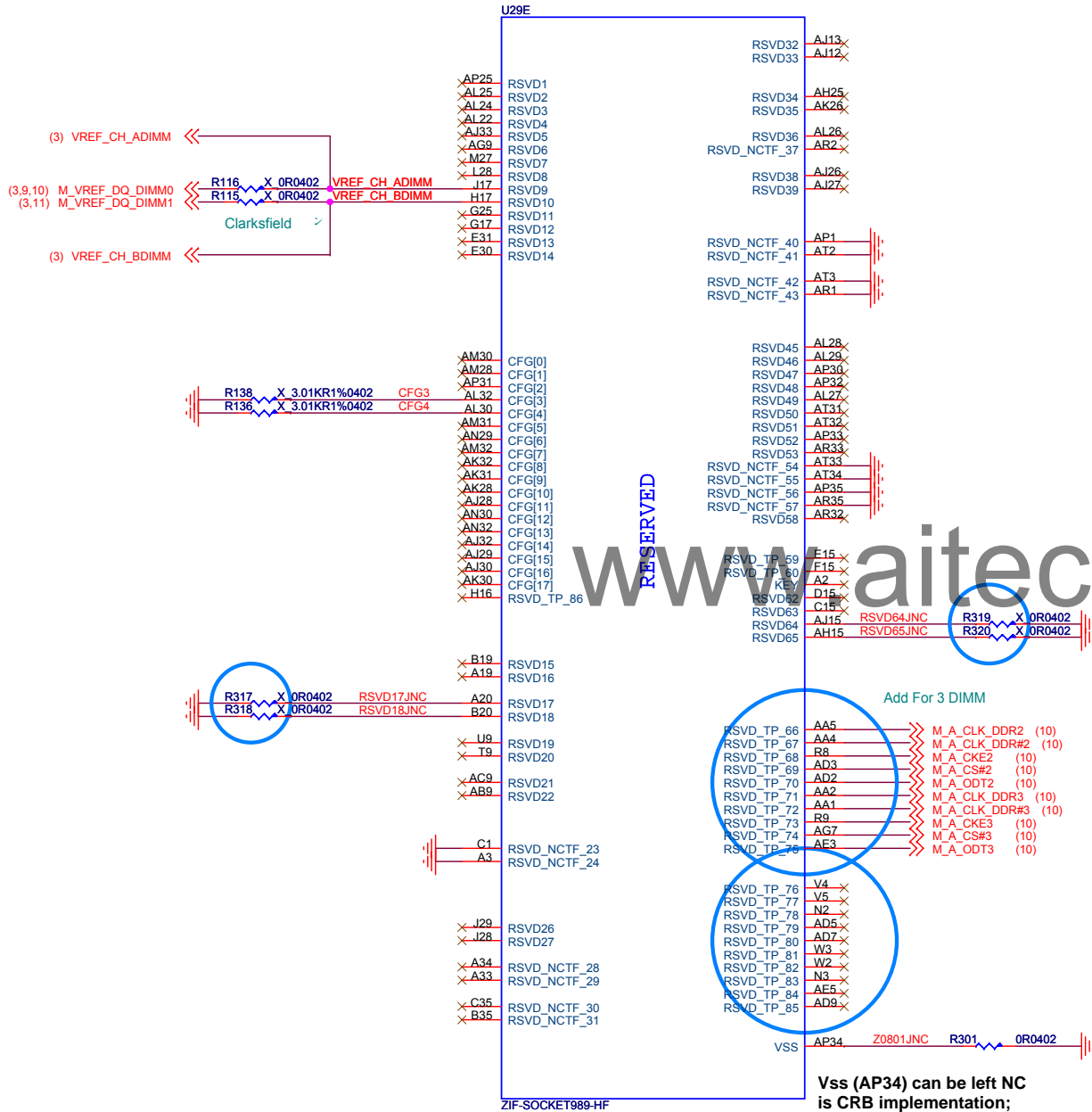


# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



Title		
PROCESSOR GND		
Size	Document Number	Rev
Custom	MS-16F1	1.1
Date:	Monday, March 29, 2010	Sheet 7 of 54

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED)



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

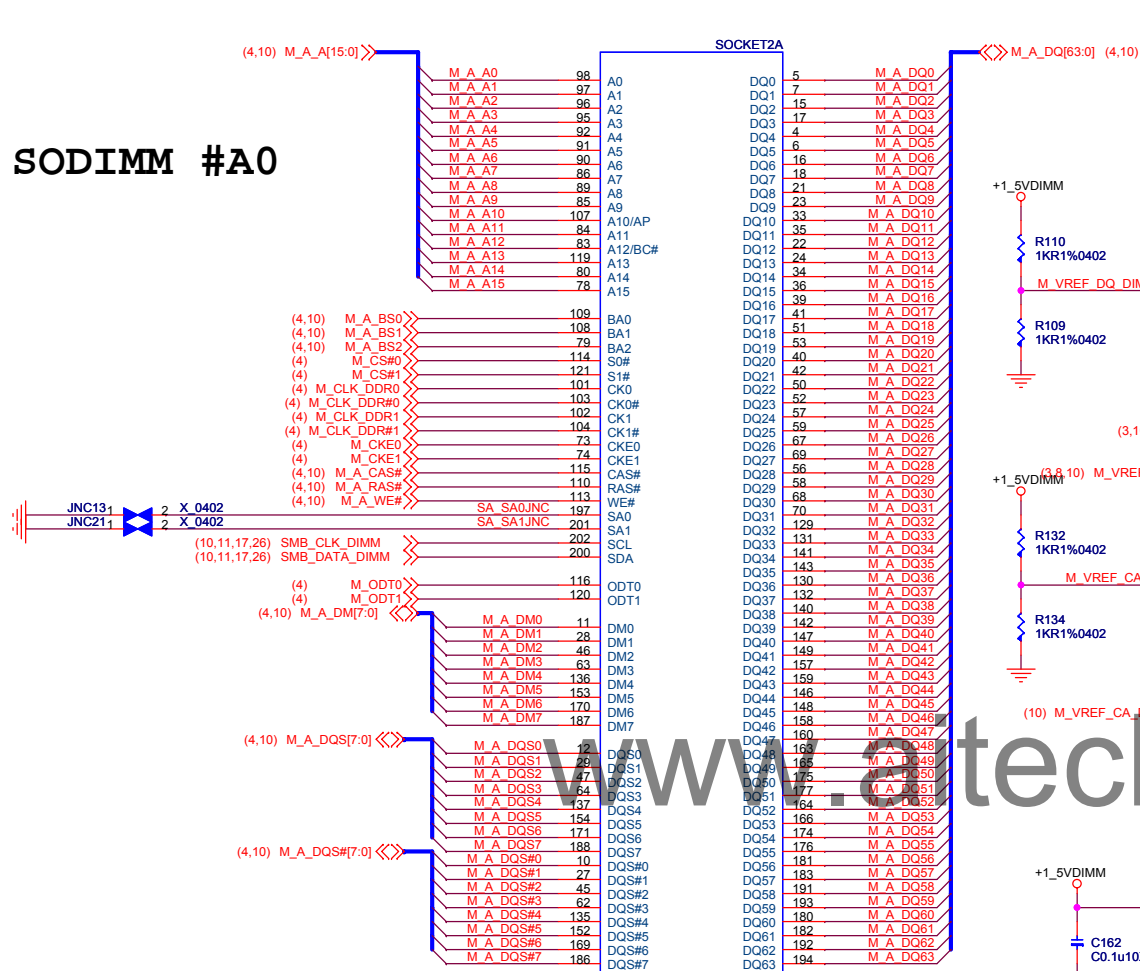
Add For 3 DIMM

**Vss (AP34) can be left NC  
is CRB implementation;  
EDS/DG recommendation to GND**

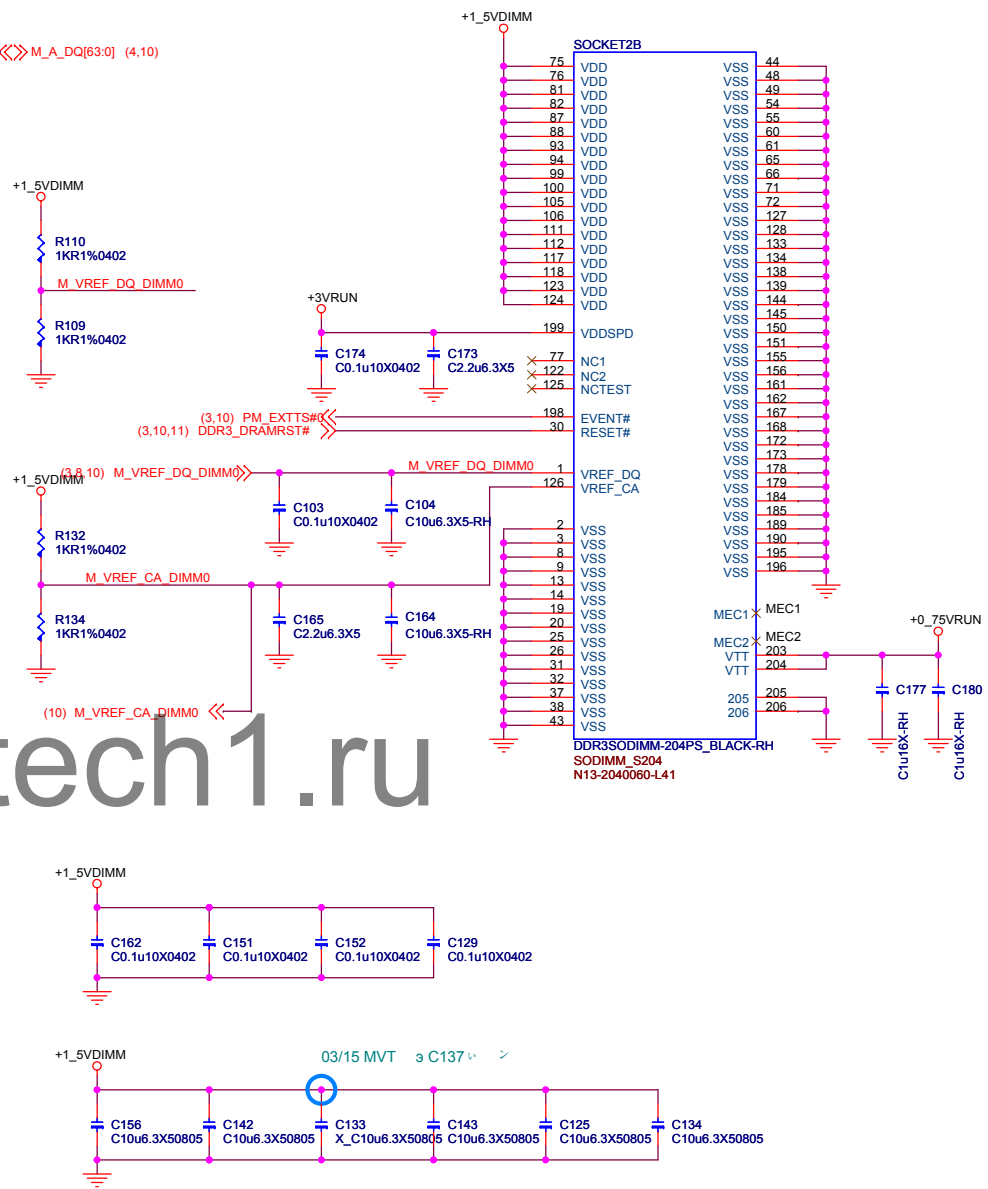
Title			
<b>PROCESSOR RESERVED</b>			
Size	Document Number	Rev	
Custom	<b>MS-16F1</b>	1.1	
Date:	Monday, March 29, 2010	Sheet	8 of 54



# SODIMM #A0

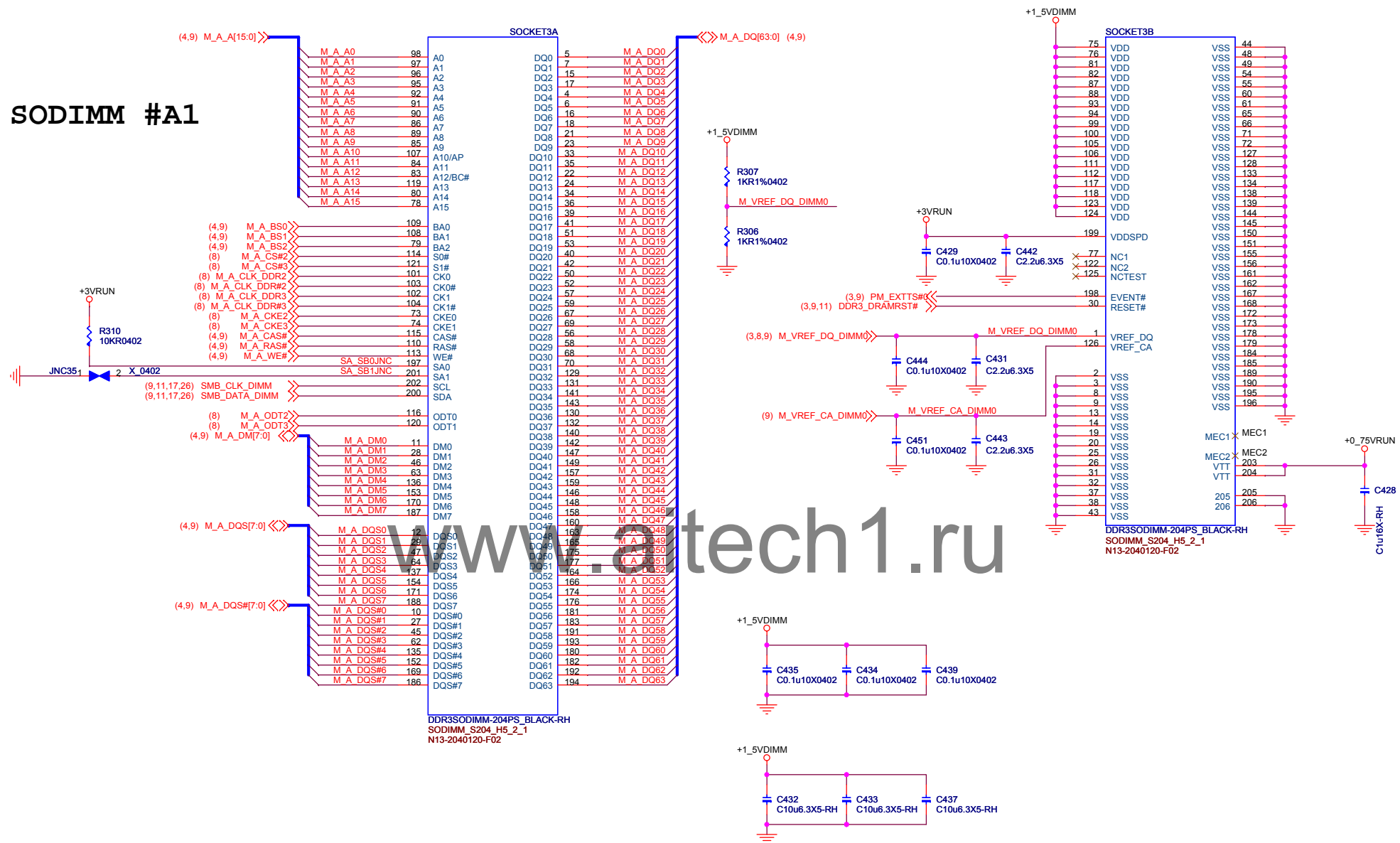


DDR3SODIMM-204PS\_BLACK-RH  
SODIMM\_S204  
N13-2040060-L41



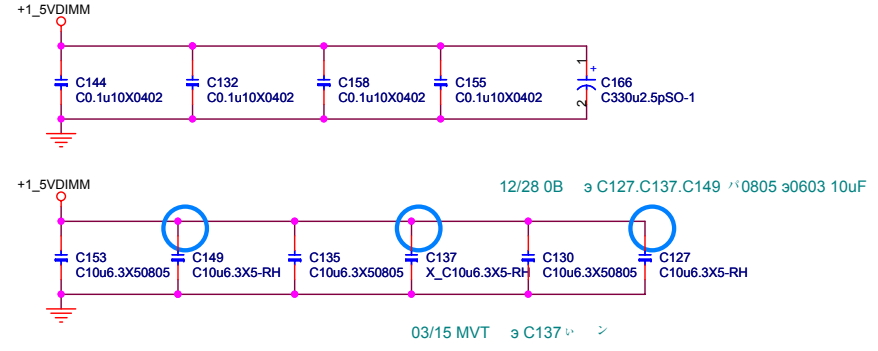
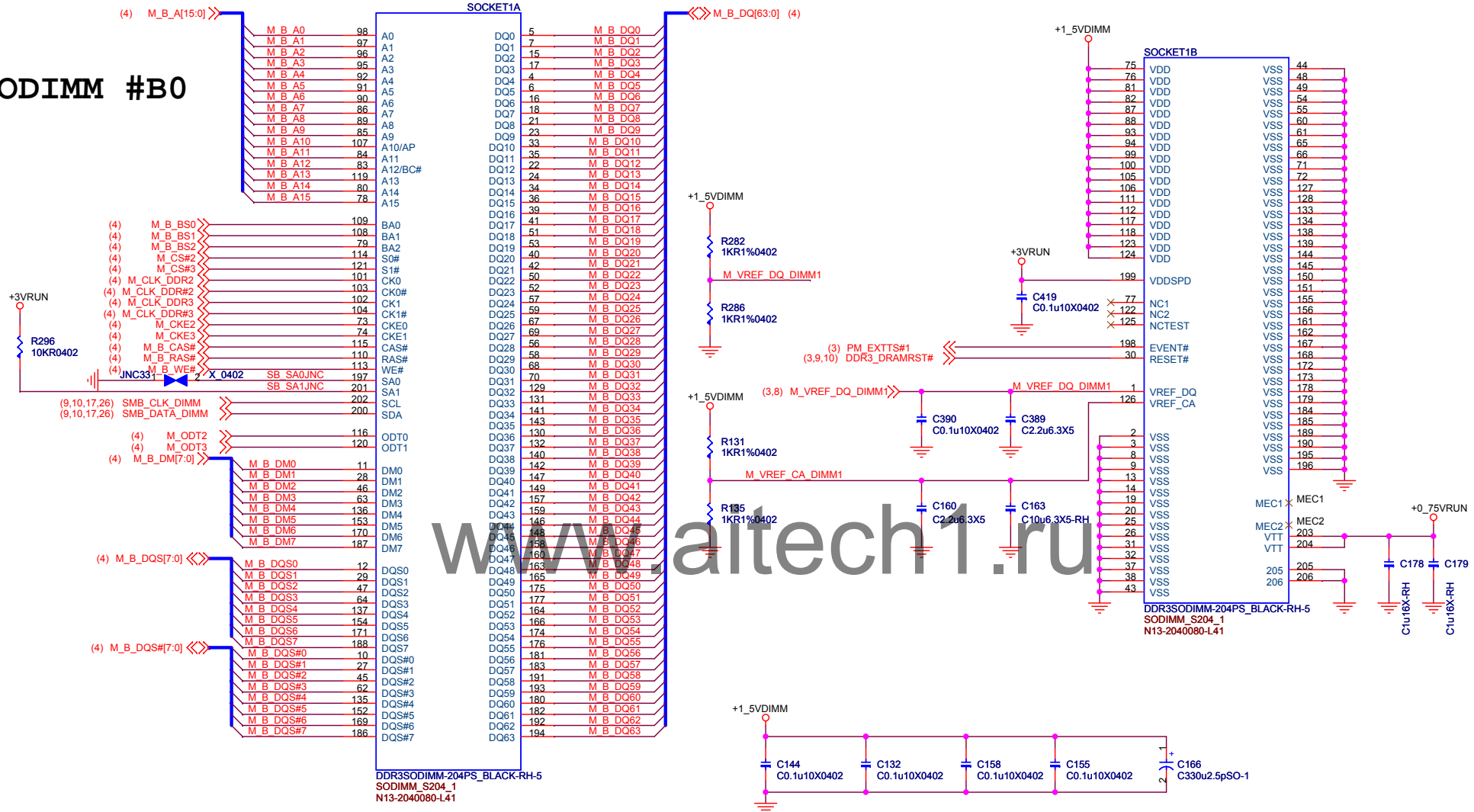
Title			DDR3 SODIMM A0	
Size	Document Number			Rev
Custom	MS-16F1			1.1
Date:	Monday, March 29, 2010	Sheet	9 of 54	

**SODIMM #A1**



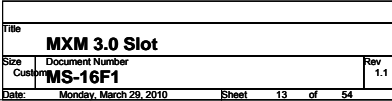
Title				
DDR3 SODIMM A1				
Size	Document Number			Rev
Custom	MS-16F1			1.1
Date:	Monday, March 29, 2010	Sheet	10	of 54

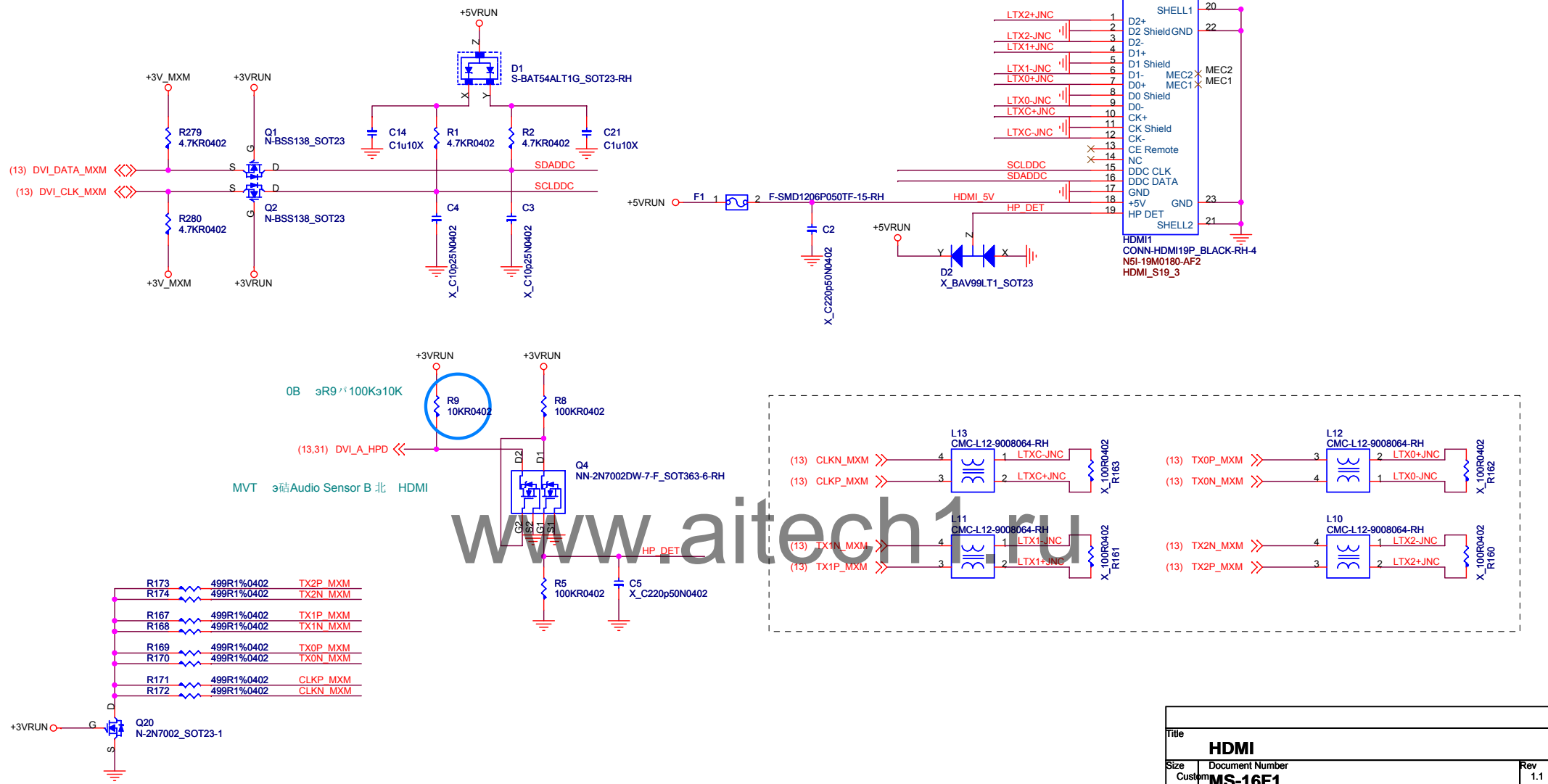
# SODIMM #B0



Title		
DDR3 SODIMM B0		
Size	Document Number	Rev
Custom	MS-16F1	1.1
Date:	Monday, March 29, 2010	Sheet 11 of 54





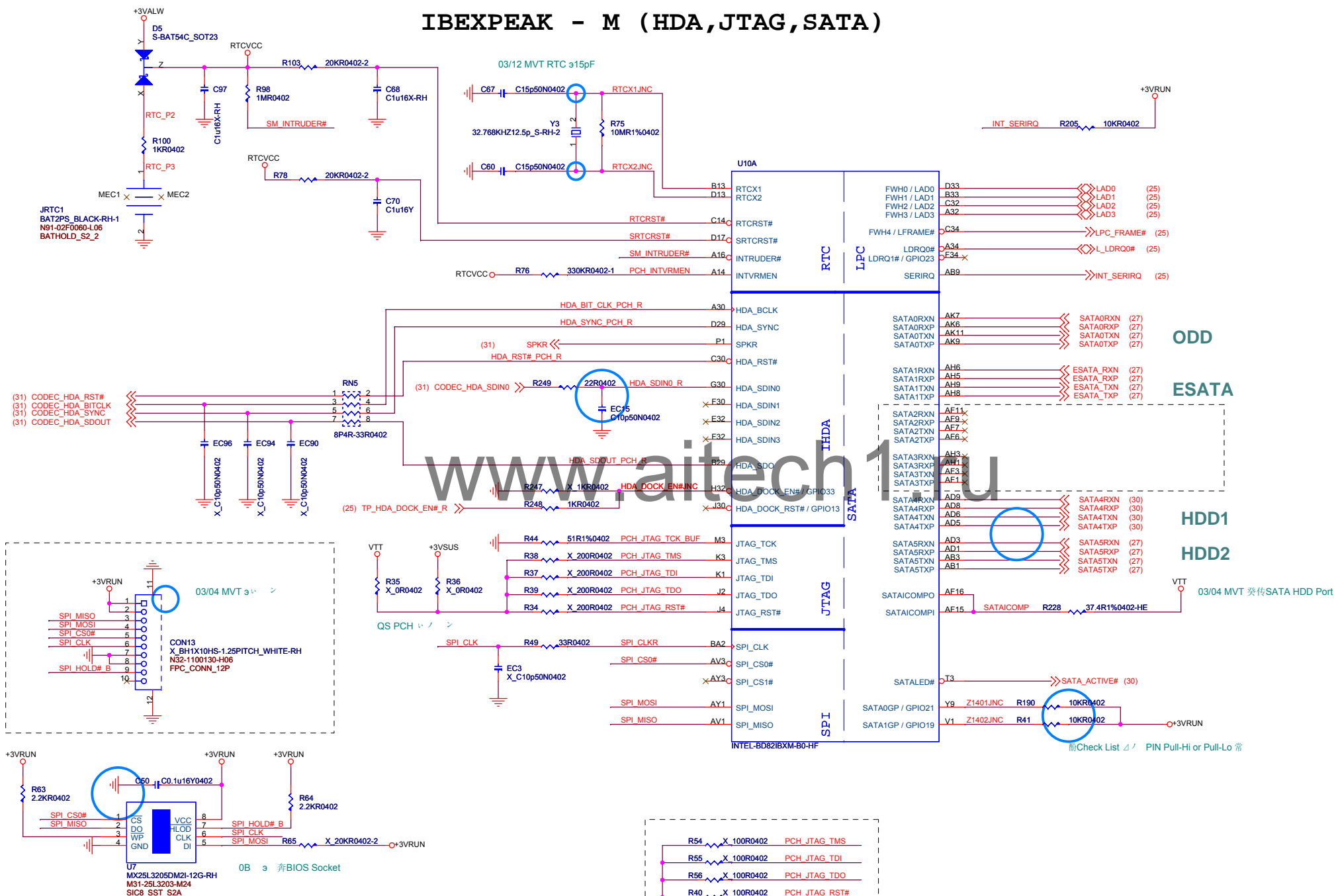


Title				
<b>HDMI</b>				
Size	Document Number			Rev 1.1
Custom	<b>MS-16F1</b>			
Date:	Monday, March 29, 2010	Sheet	14 of 54	



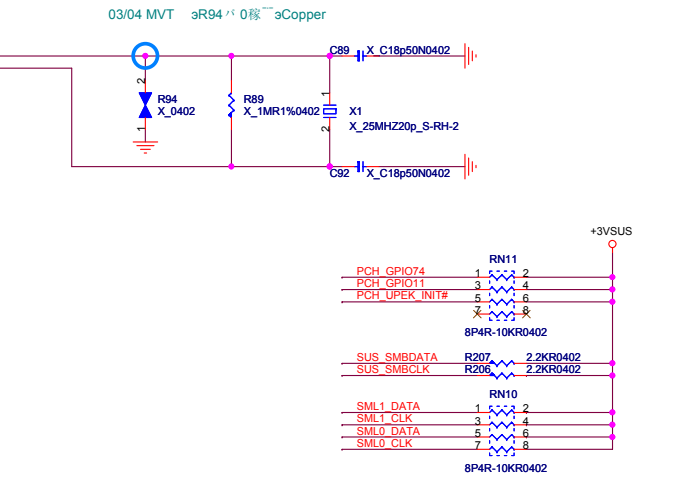
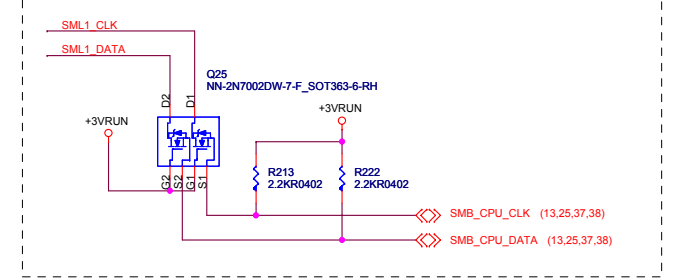
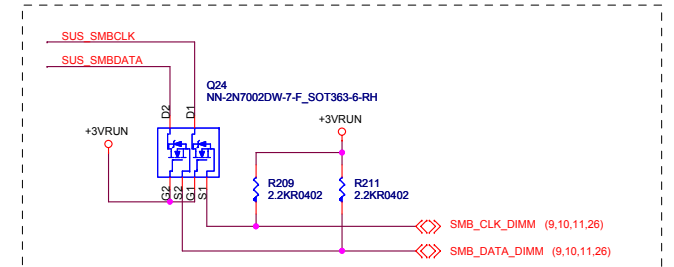
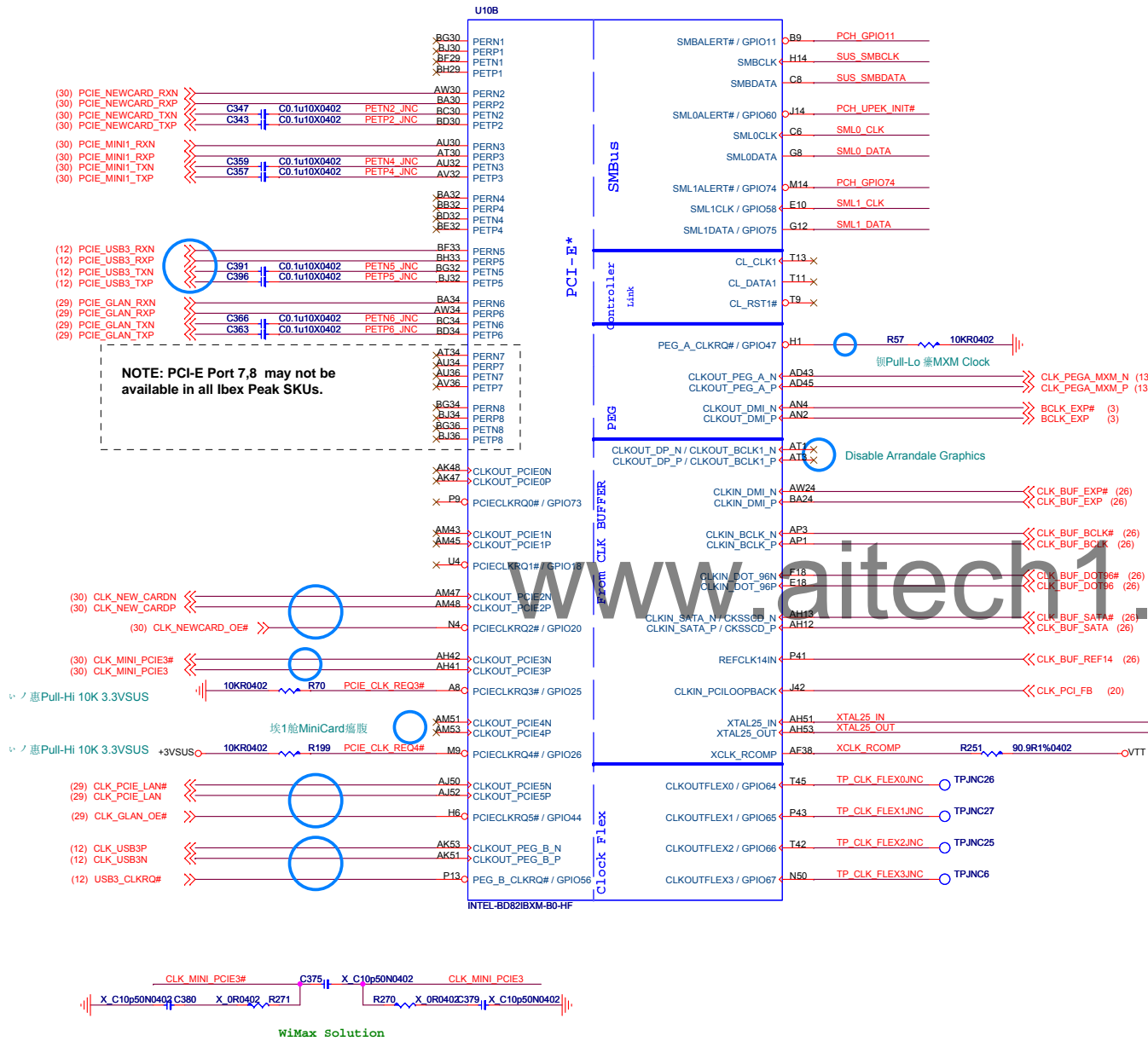


# IBEXPEAK - M (HDA,JTAG,SATA)



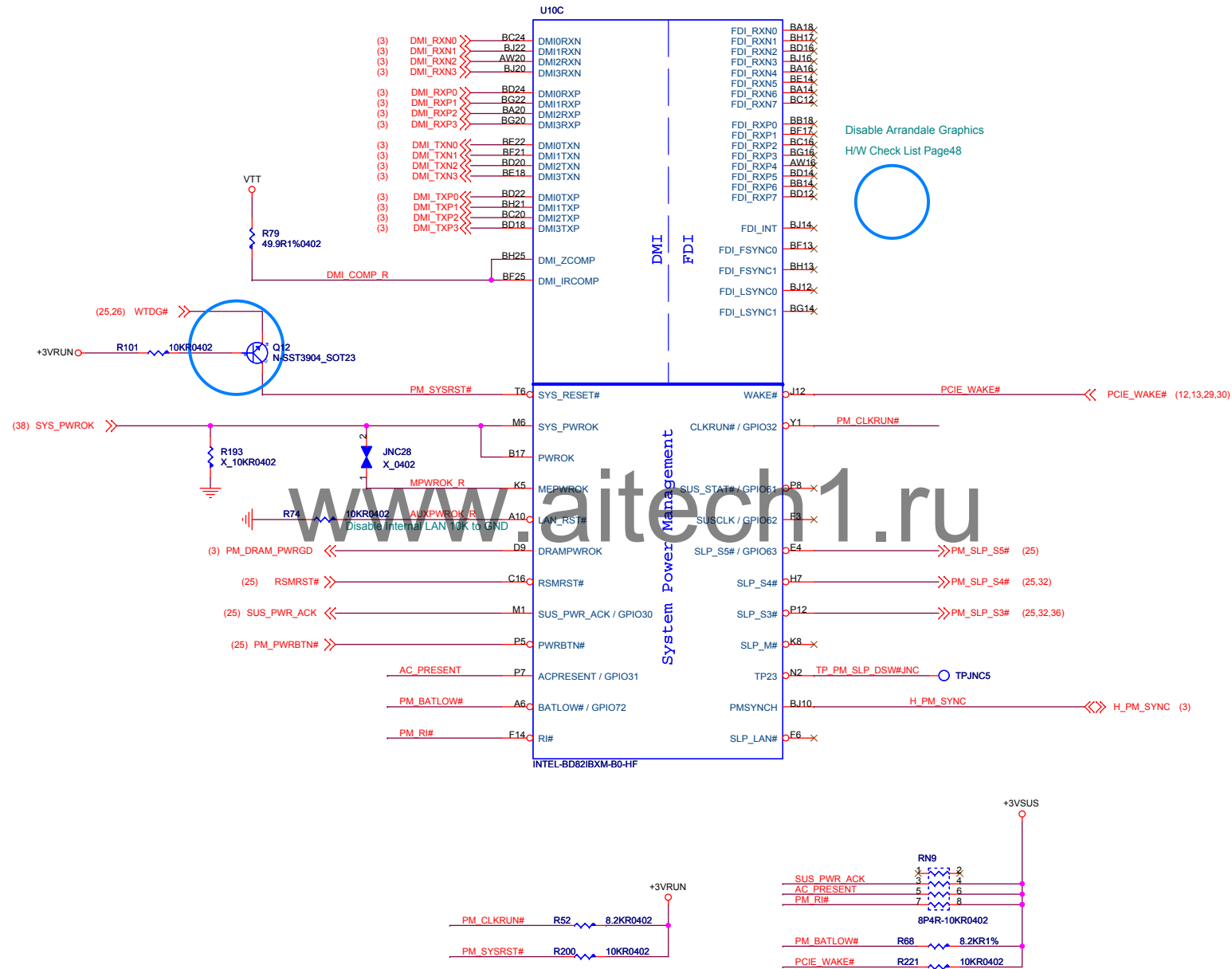


# IBEXPEAK - M (PCI-E, SMBUS, CLK)

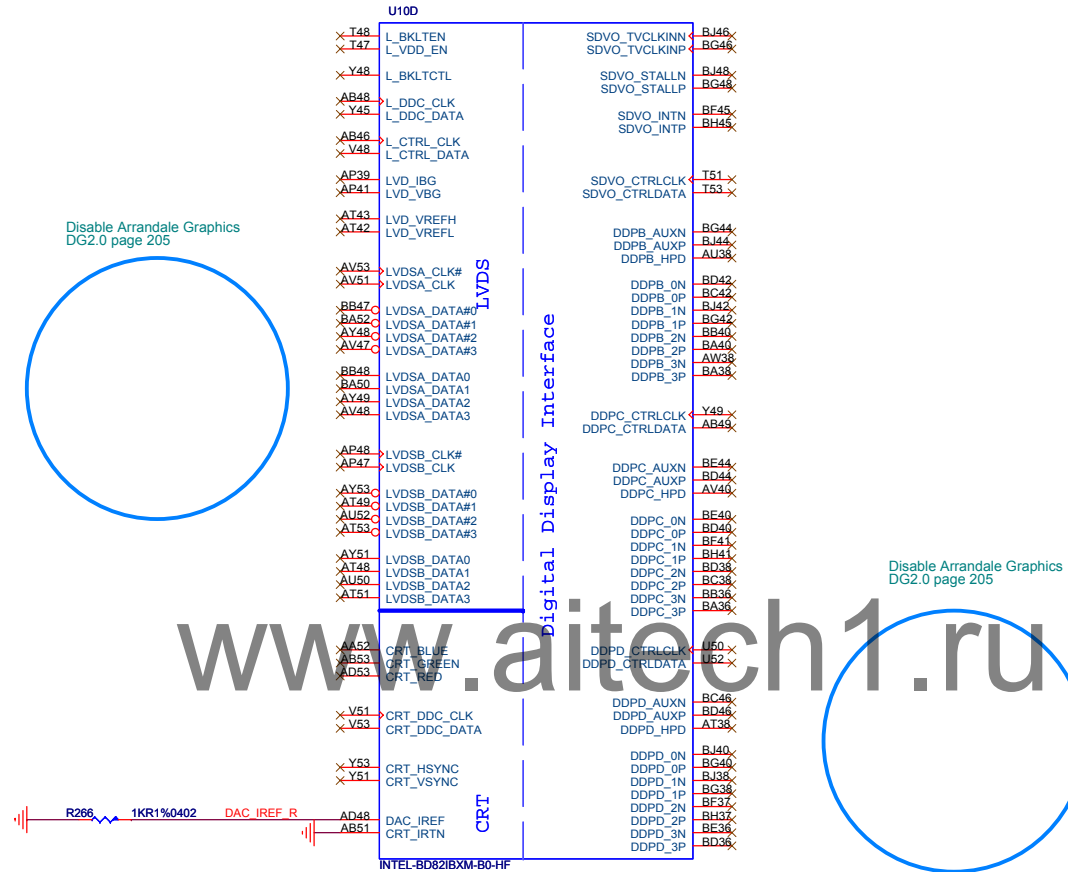


Title			
PCH_PCIE/SMBUS/CLK			
Size	Document Number		Rev
Custom	MS-16F1		1.1
Date:	Monday, March 29, 2010	Sheet	17 of 54

# IBEXPEAK - M (DMI, FDI, GPIO)

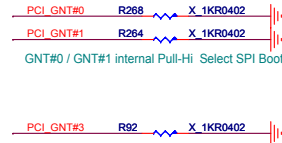
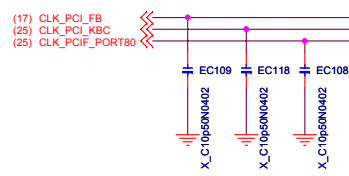
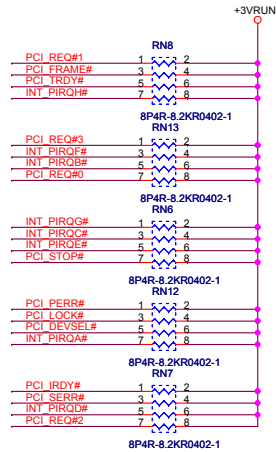


# IBEXPEAK - M (LVDS,DDI)

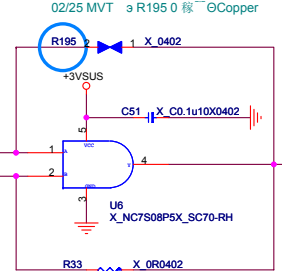
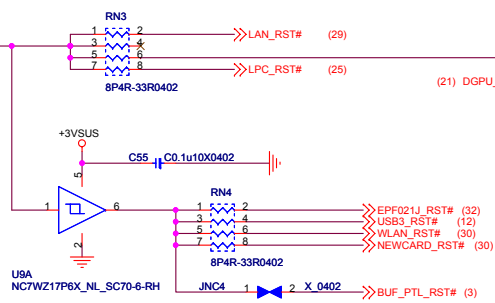
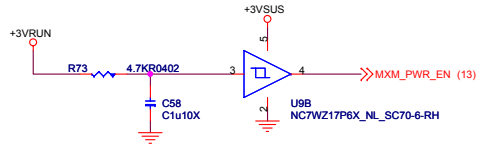
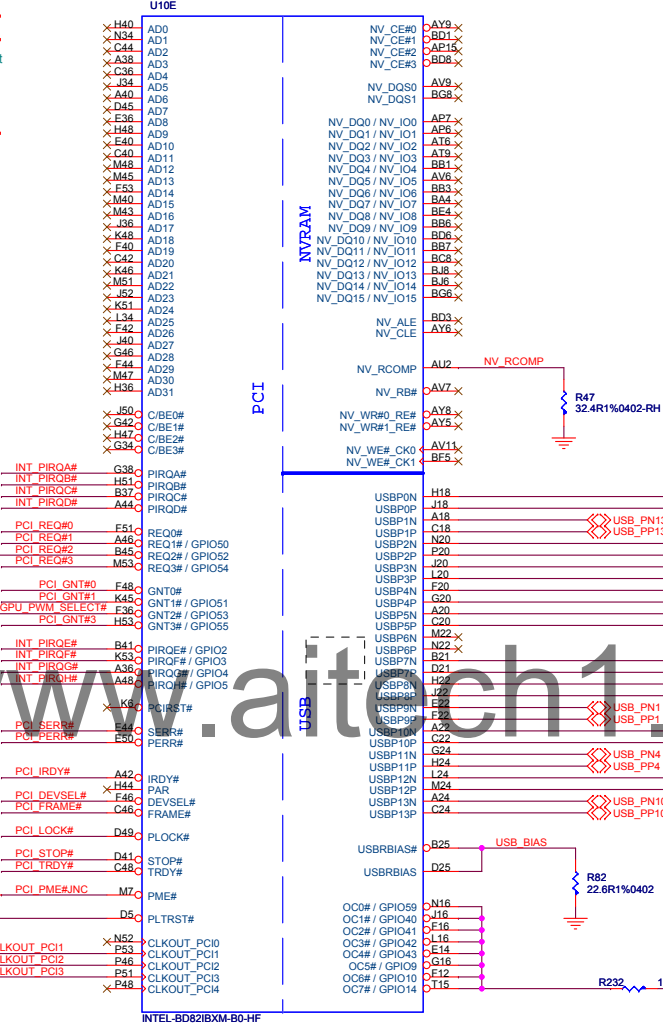


# IBEXPEAK - M (PCI,USB,NVRAM)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



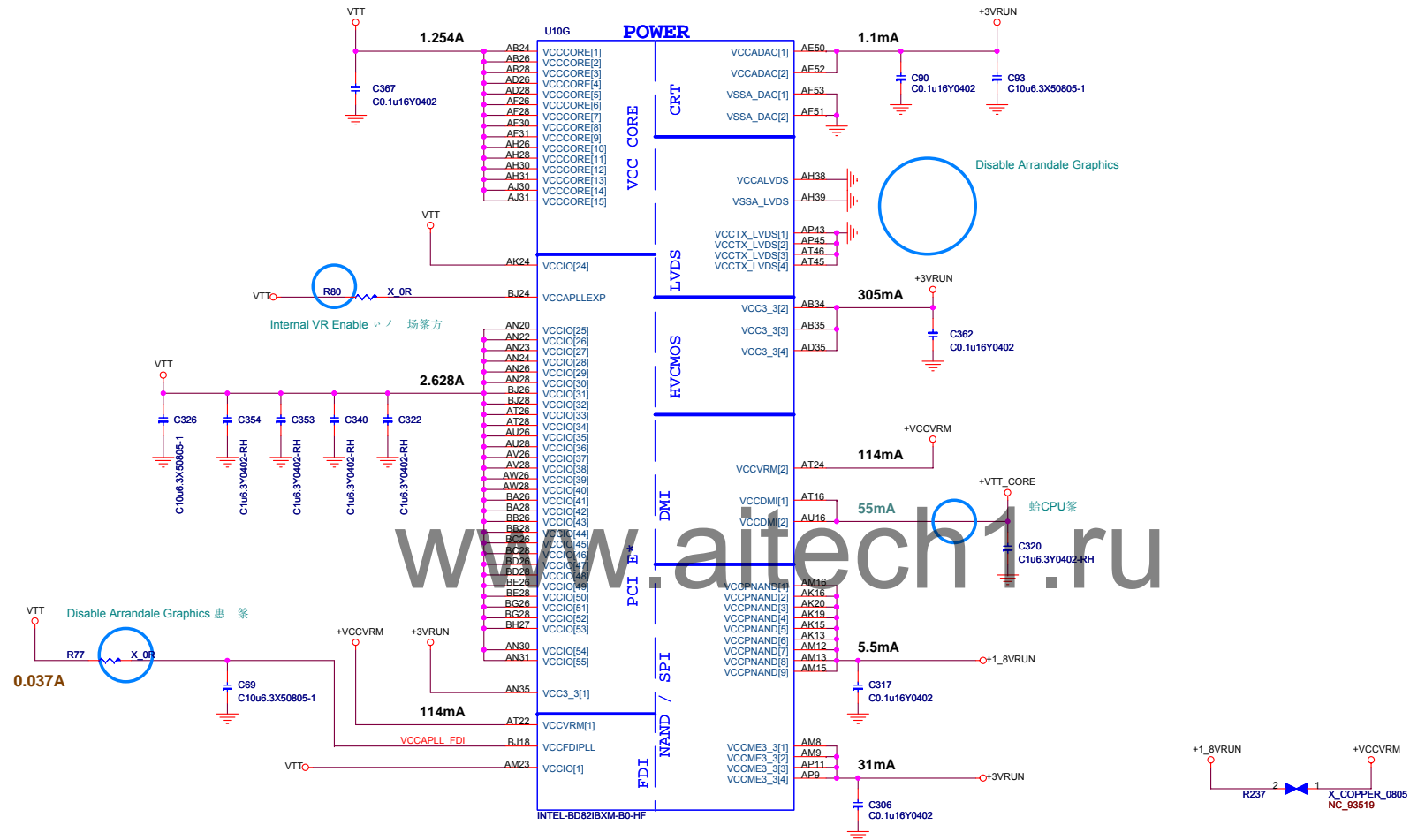
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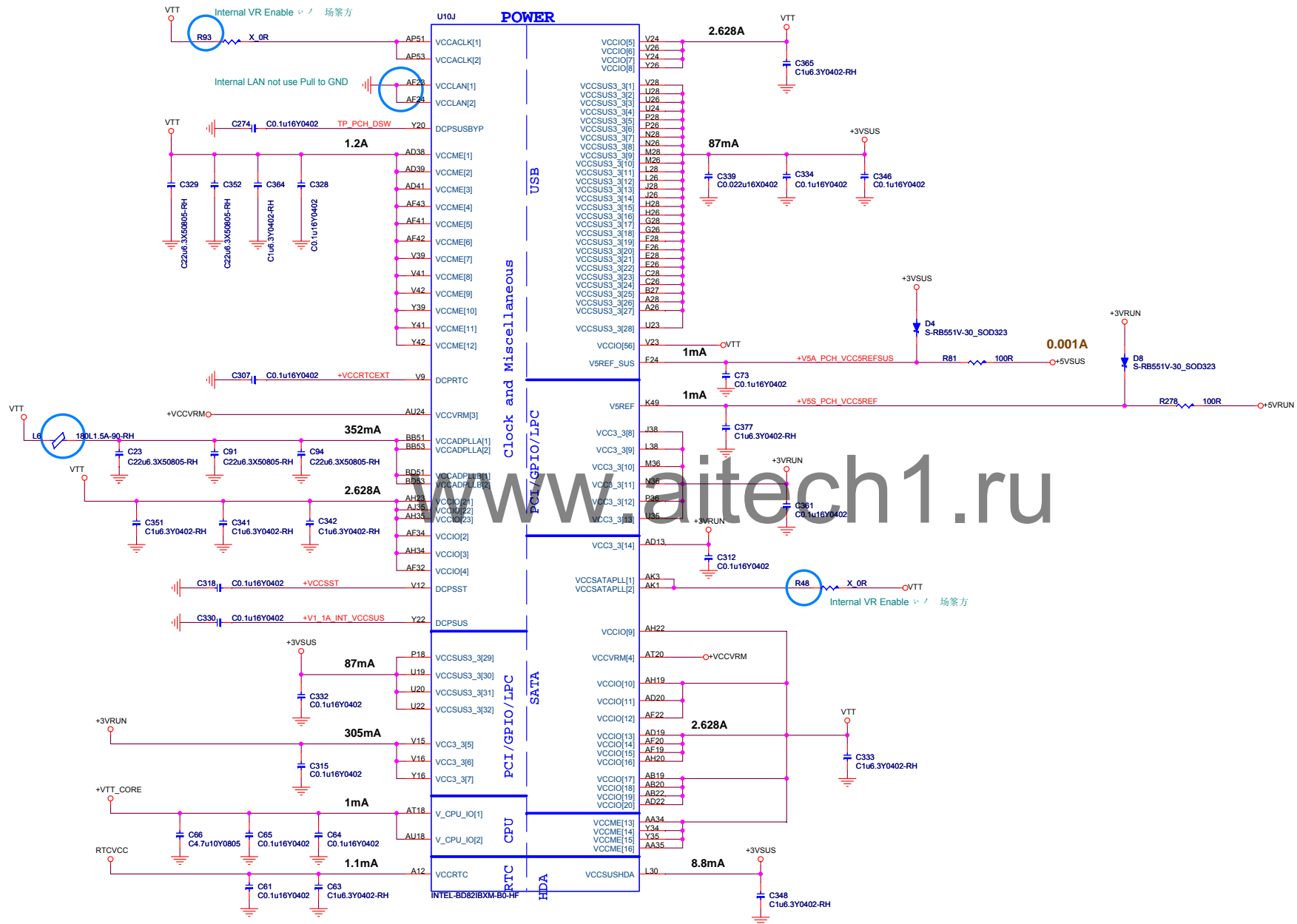
Title		
PCH_PCI/USB/NVRAM		
Size	Document Number	Rev
Custom	MS-16F1	1.1
Date:	Monday, March 29, 2010	Sheet 20 of 54

# IBEXPEAK - M (GPIO,VSS\_NCTF,RSVD)

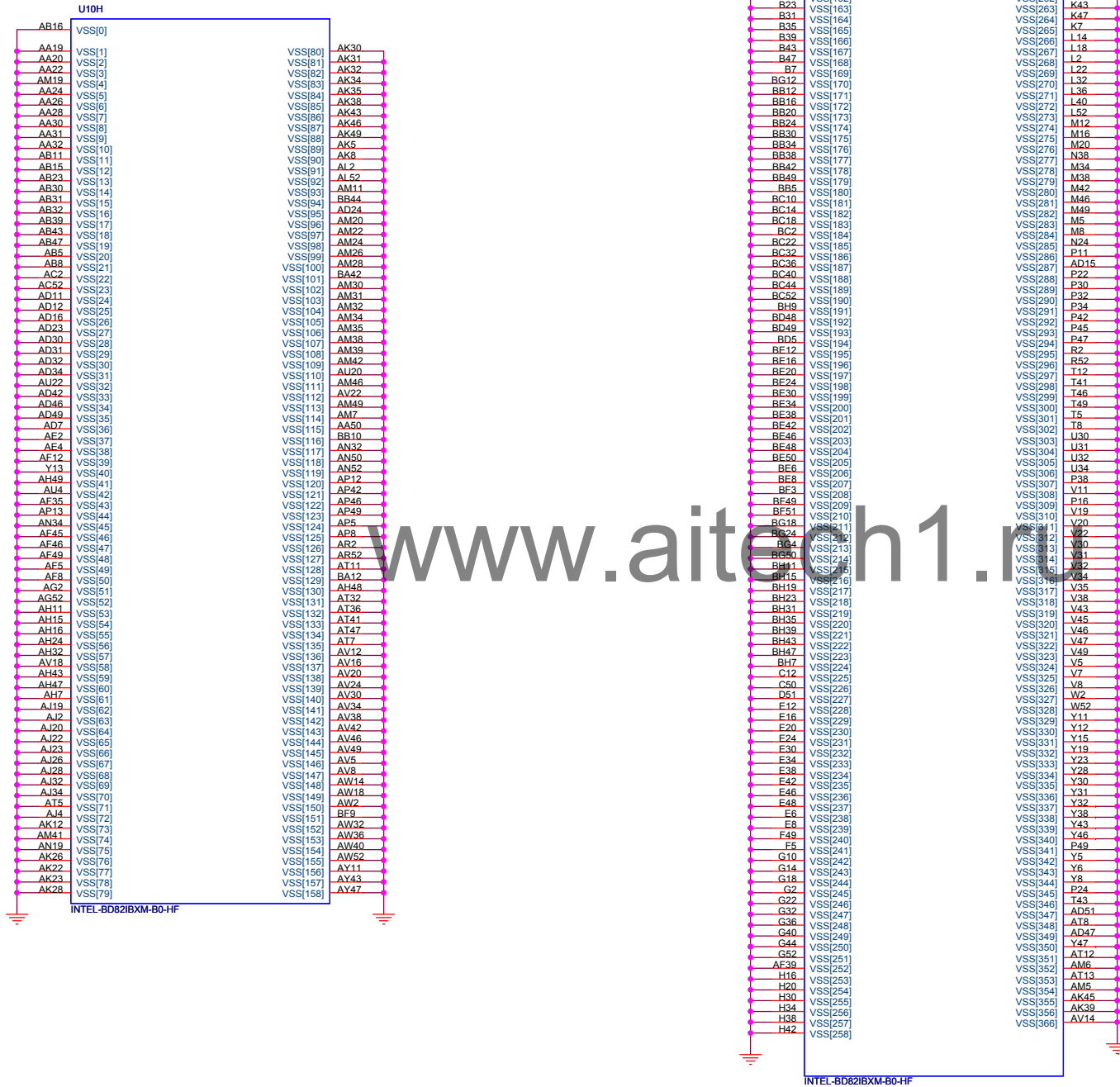


**IBEXPEAK - M (POWER)**

# IBEXPEAK - M (POWER)

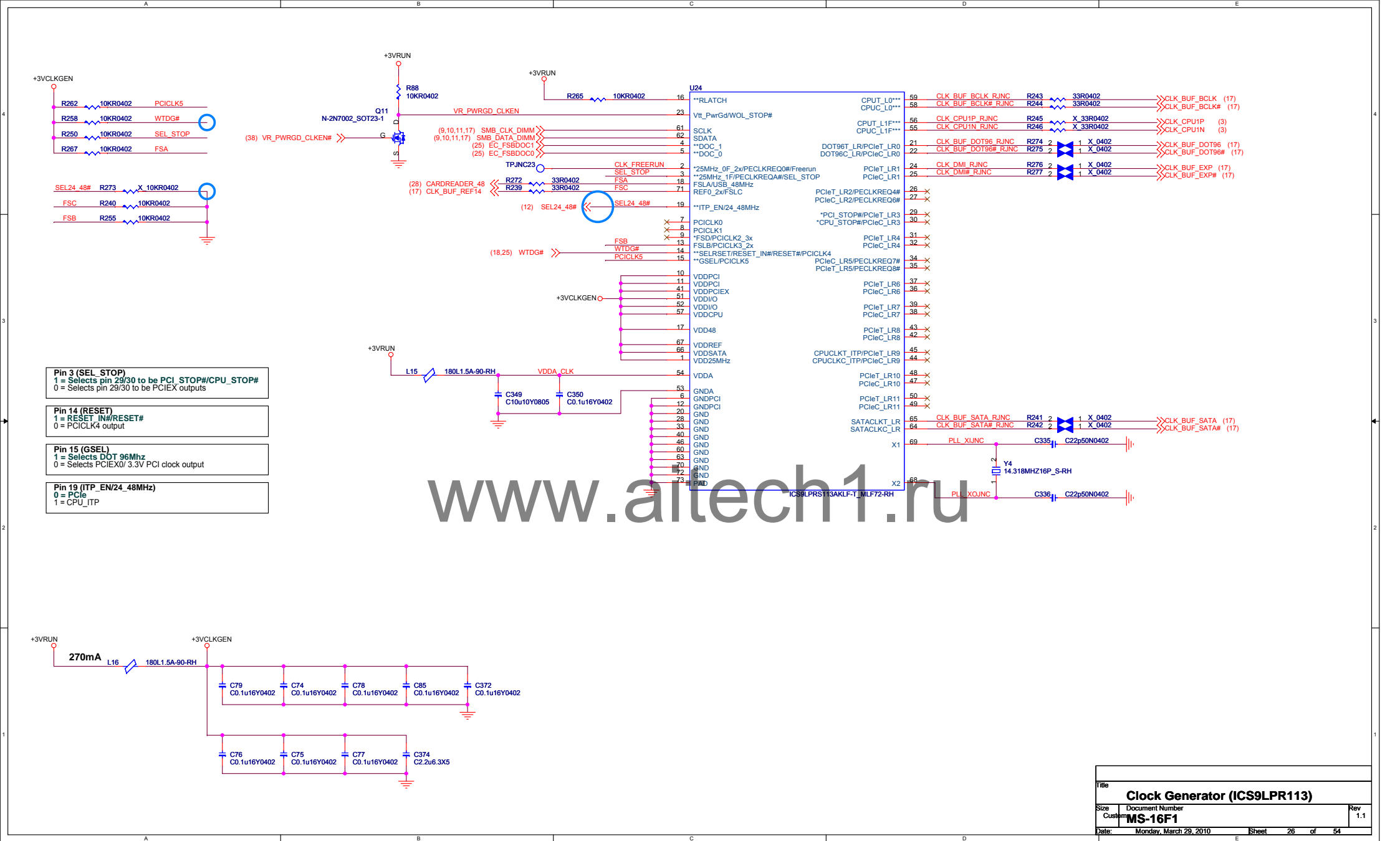


**IBEXPEAK - M (GND)**





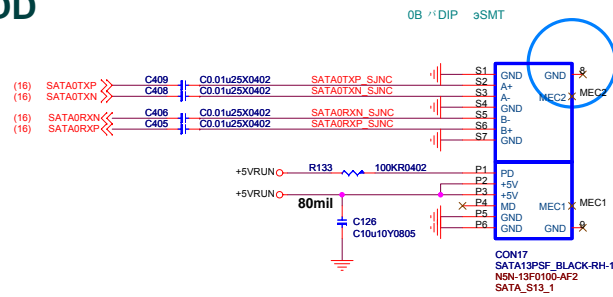




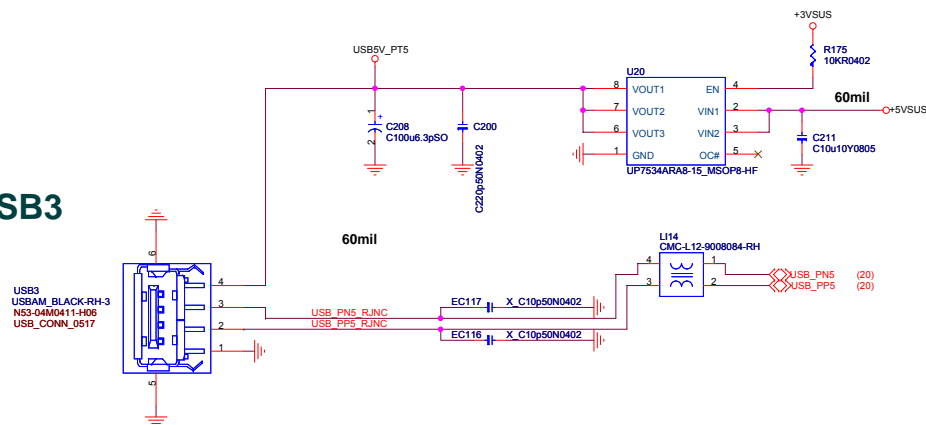
- Pin 3 (SEL\_STOP)**  
1 = Selects pin 29/30 to be PCI\_STOP#/CPU\_STOP#  
0 = Selects pin 29/30 to be PCIe outputs
- Pin 14 (RESET)**  
1 = RESET\_IN#/RESET#  
0 = PCICLK4 output
- Pin 15 (GSEL)**  
1 = Selects DOT 96MHz  
0 = Selects PCIe0/ 3.3V PCI clock output
- Pin 19 (ITP\_EN/24\_48MHz)**  
1 = CPU\_ITP

Title			
Clock Generator (ICS9LPR113)			
Size	Document Number	Rev	
Custom	MS-16F1	1.1	
Date:	Monday, March 29, 2010	Sheet	26 of 54

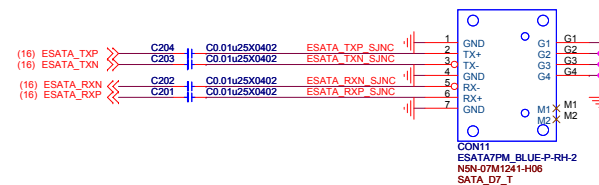
## ODD



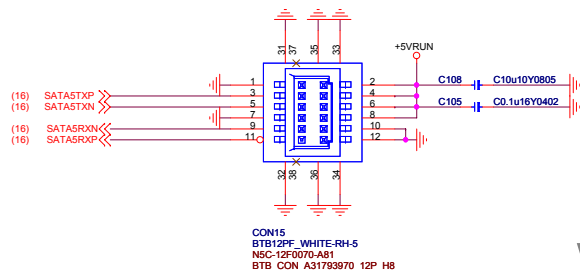
## USB3



## ESATA



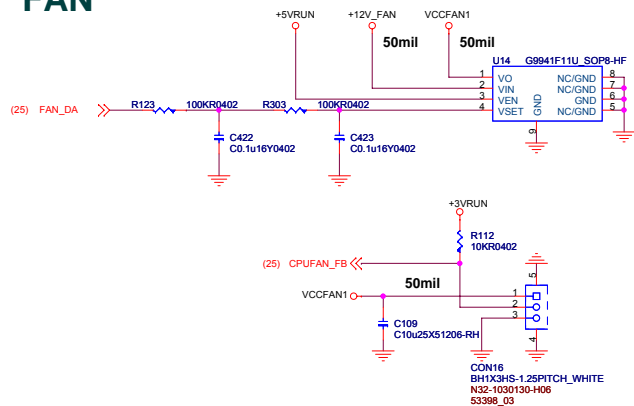
## SATA HDD2



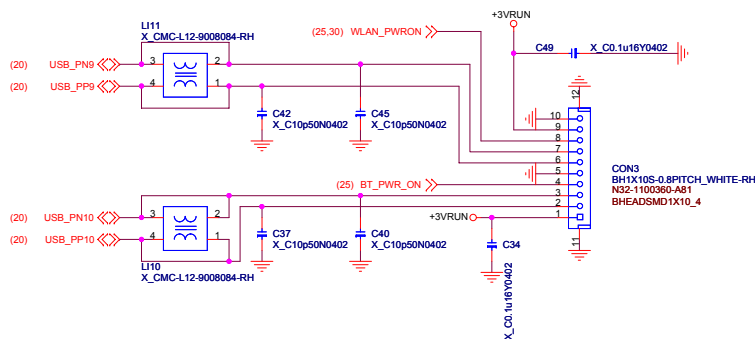
## BT (3801)

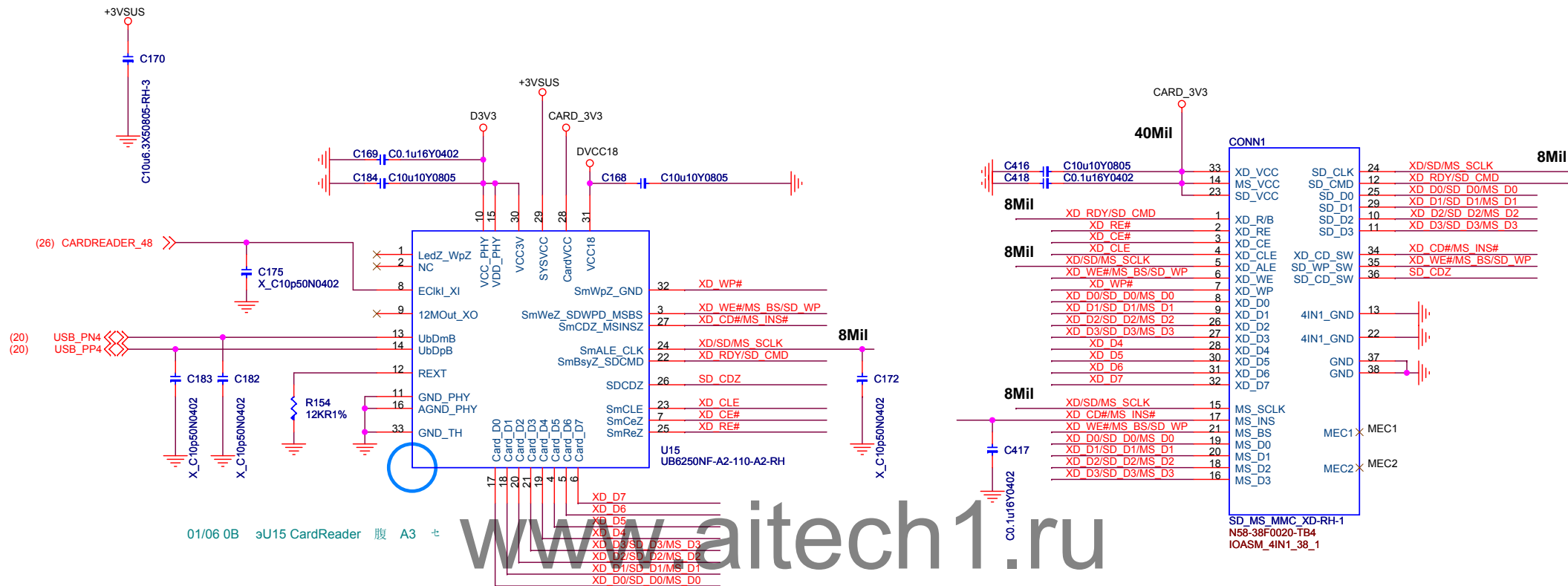
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## FAN



## WLAN/BT (3870)

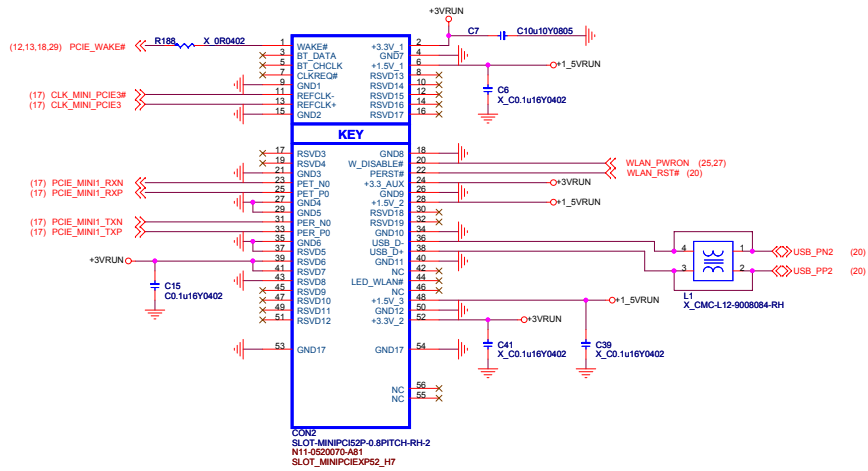




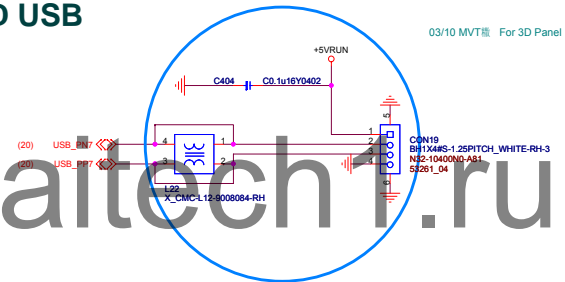
Title		
CARD READER(UB6250)		
Size	Document Number	Rev
Custom	MS-16F1	1.1
Date:	Monday, March 29, 2010	Sheet 28 of 54



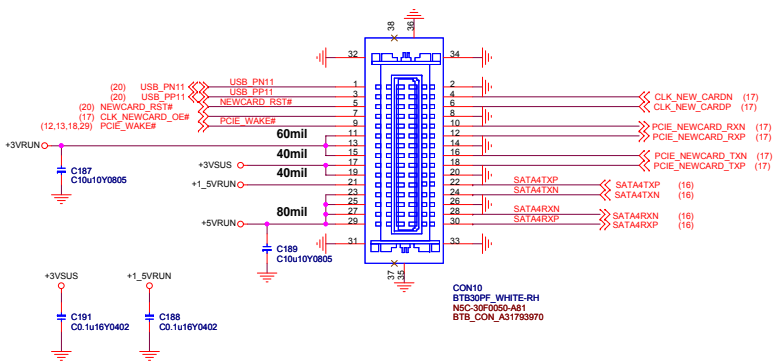
## WLAN



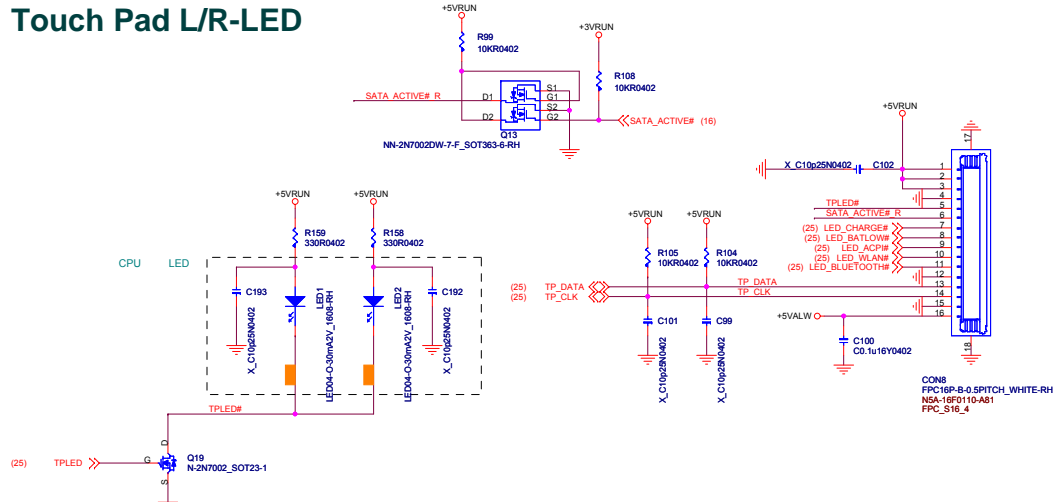
## 3D USB

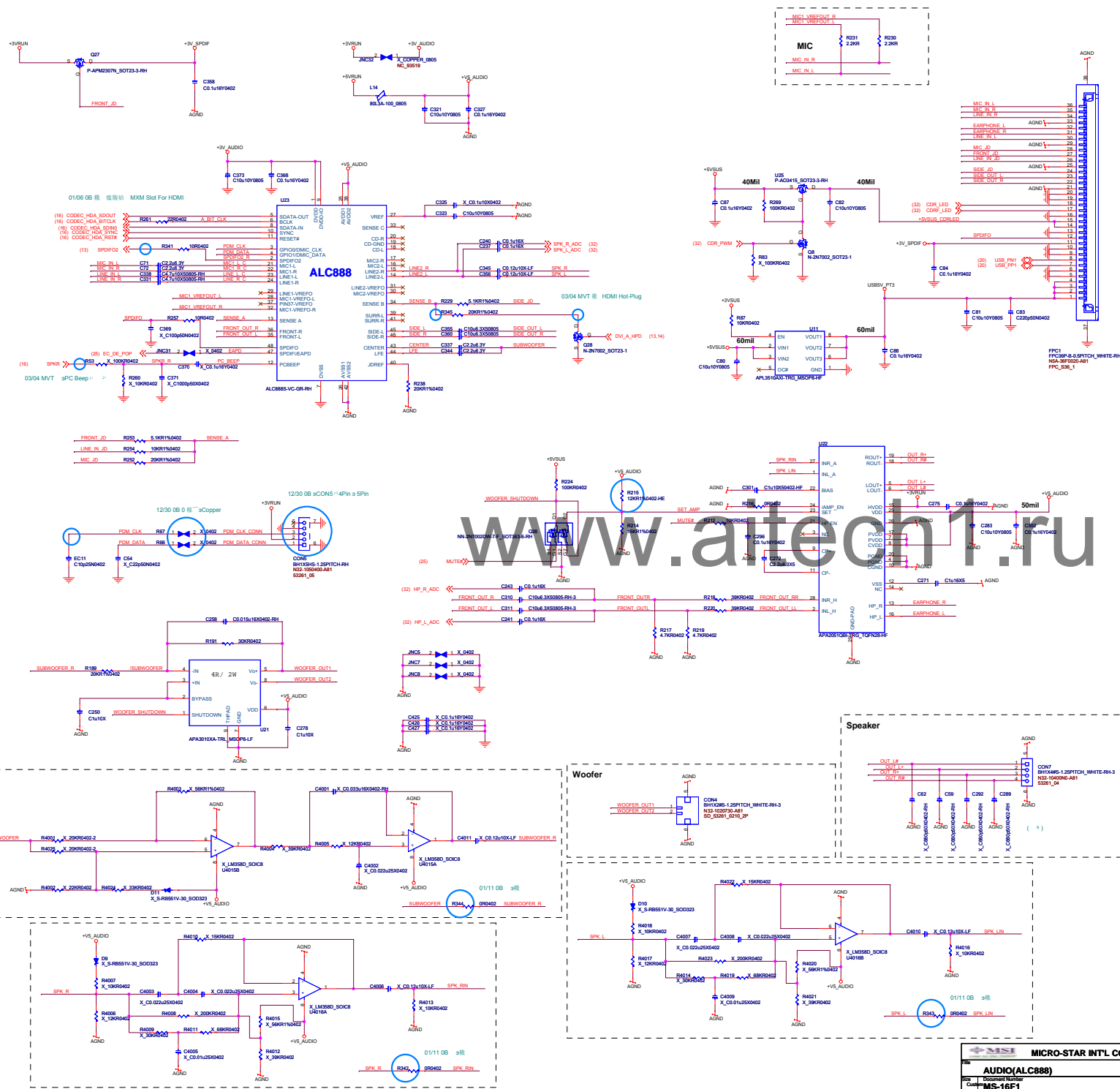


## BTB Conn



## Touch Pad L/R-LED



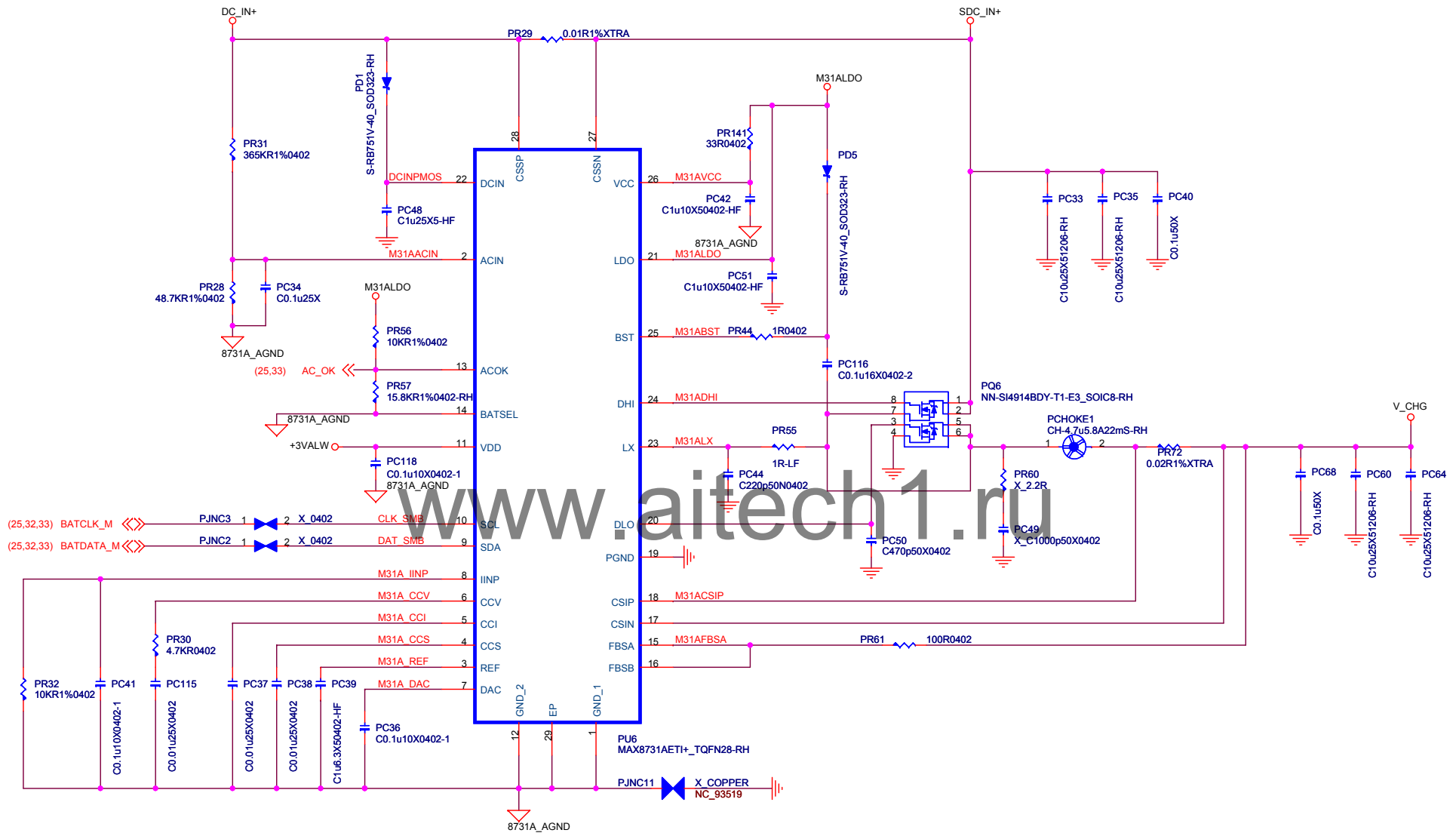








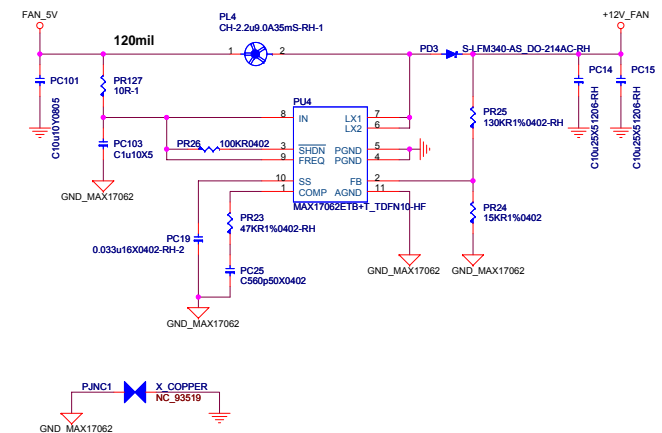
Title			
<b>Battery Select</b>			
Size	Document Number	Rev	
Custom	<b>MS-16F1</b>	1.1	
Date:	Monday, March 29, 2010	Sheet	33 of 54

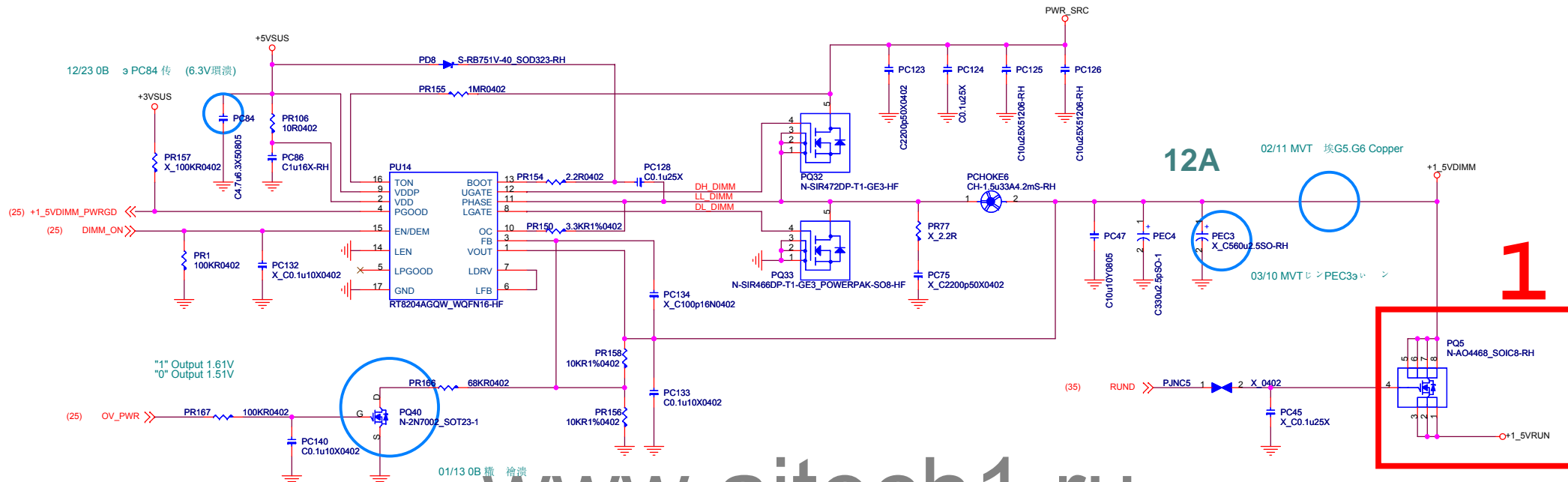


IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2.  $V\_IINP = IINPUT \times RS1 \times 3mA/V \times PR168$

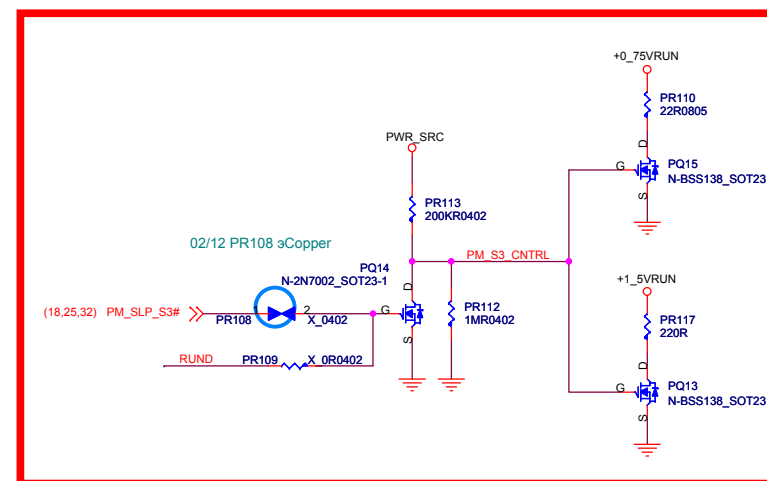
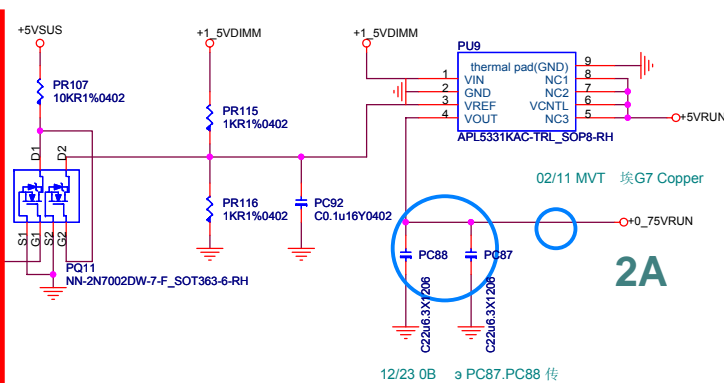
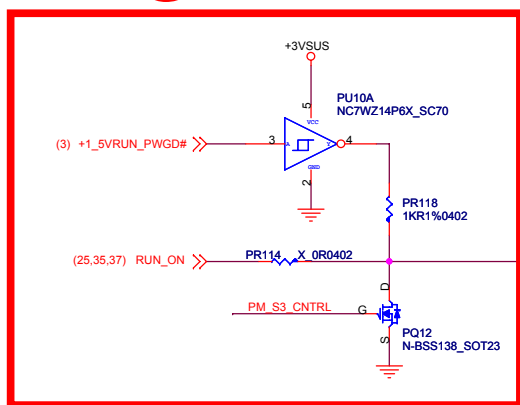
Title		
Battery Charger		
Size	Document Number	Rev
B	MS-16F1	1.1
Date:	Monday, March 28, 2010	Sheet 34 of 54





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2



PR195= 312K 3 PHASE  
412K 2 PHASE

(18) SYS\_PWR0K  
(26) VR\_PWR0G\_CLKEN

Place Pc160 across  
VW and COMP

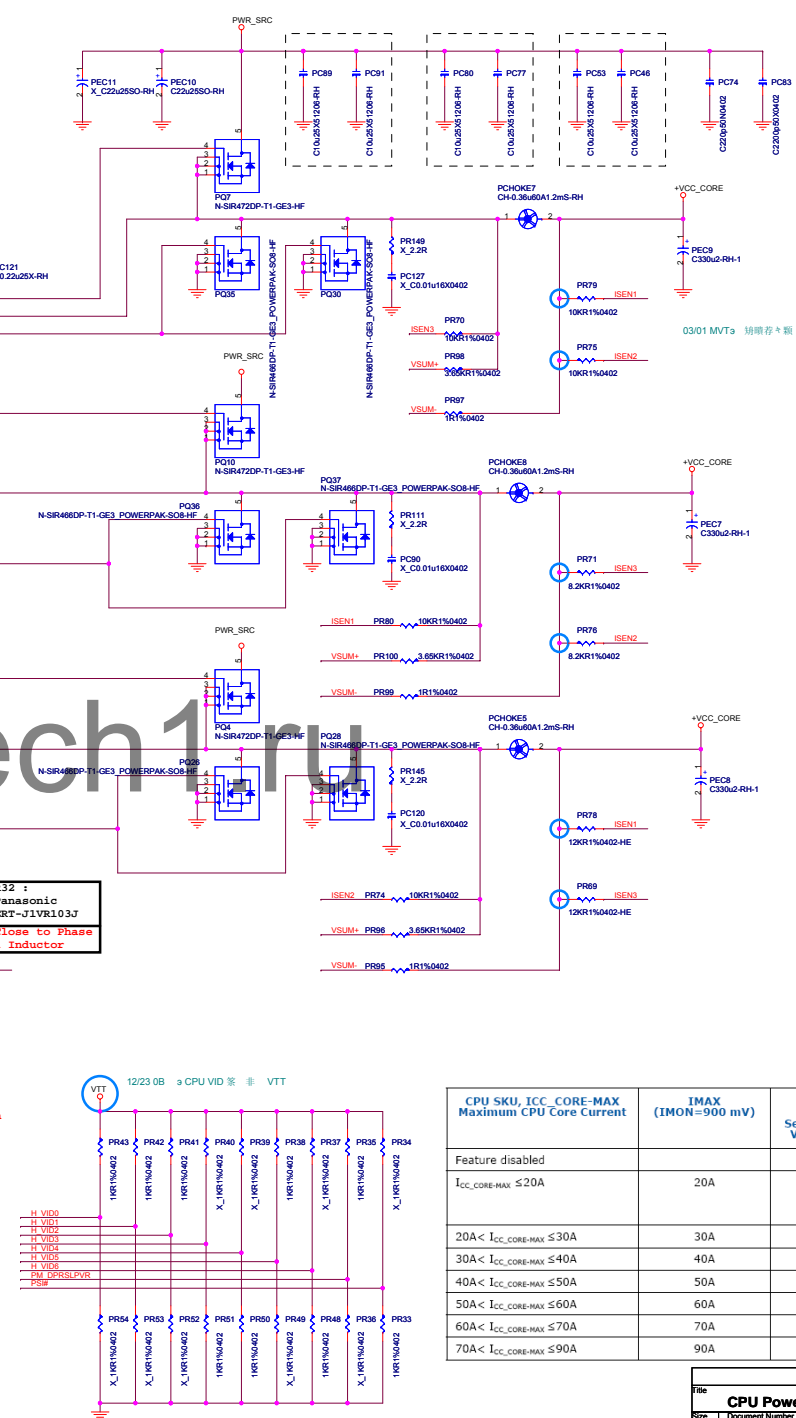
Address 0x60

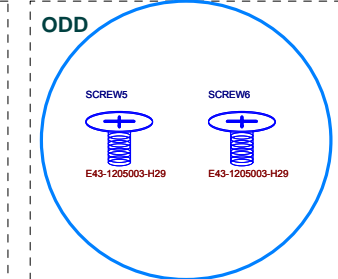
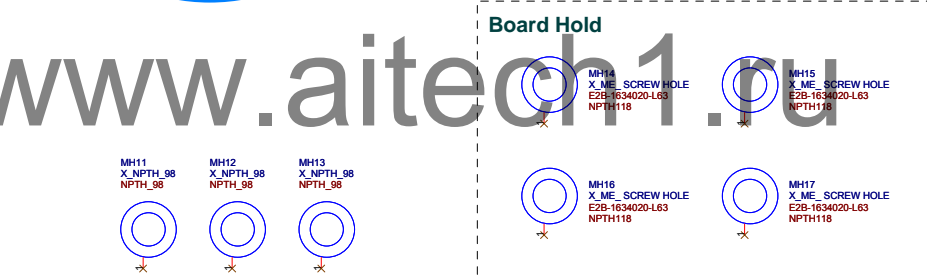
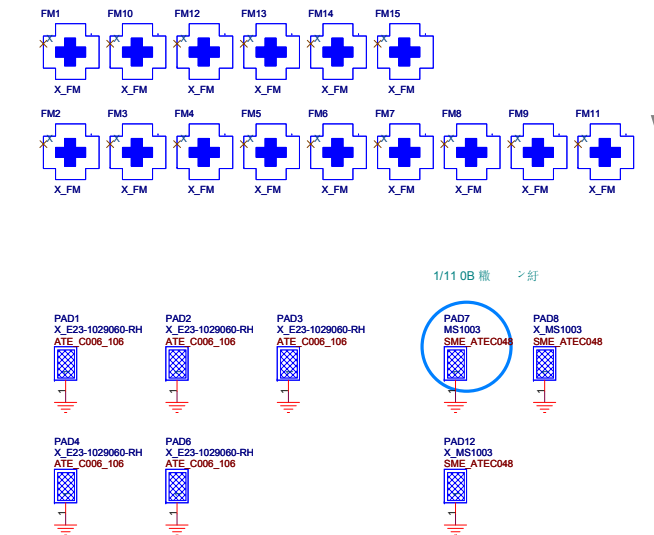
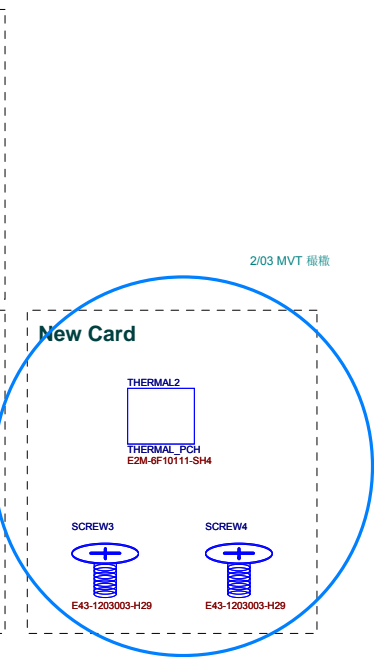
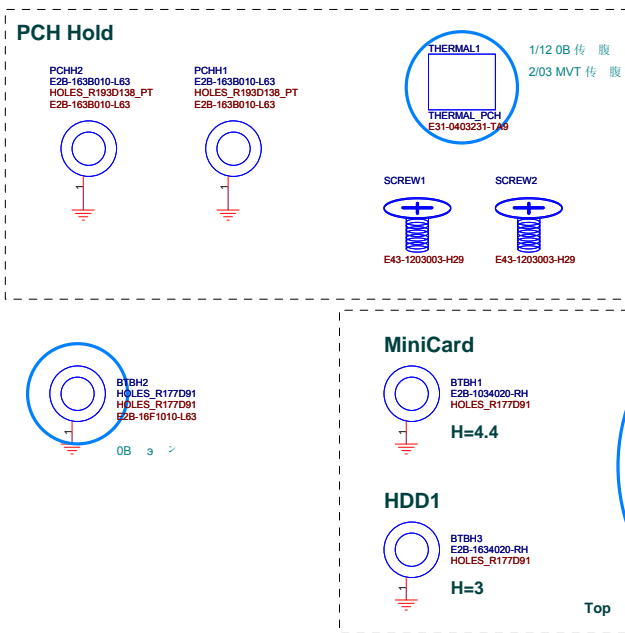
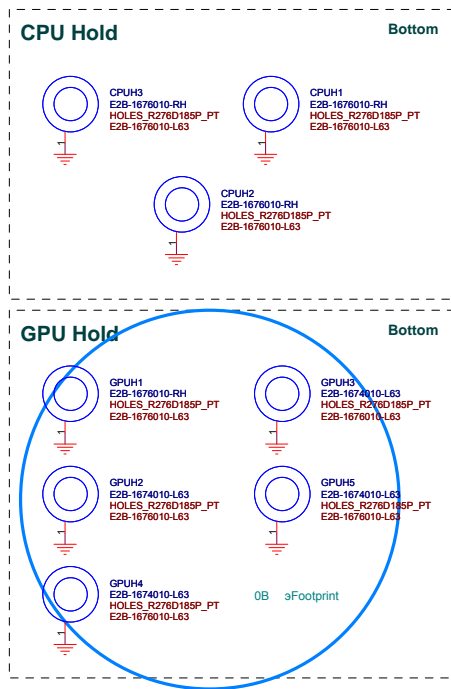
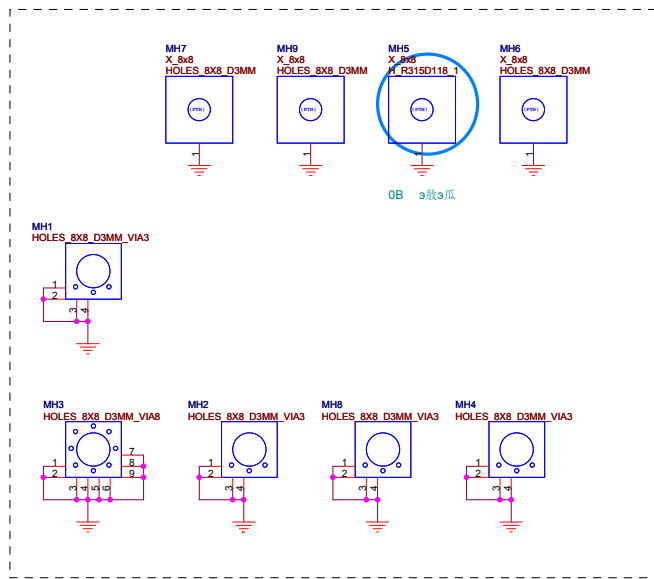
$V_{ntc} = V_{dcr} * R_{ntc} / (R_{ntc} + R_{sum})$   
where  $R_{ntc} = R_{30} * (R_{27} + R_{32}) / (R_{30} + R_{27} + R_{32})$   
 $R_{sum} = (R_8 + R_{14}) / 2$  -- 2-phase  
 $V_{dcr} = I_{out} * DCR / 2$  -- 2-phase  
Above is based on the condition of  $L/DCR = (R_{sum} // NTC) * C_n$   
where  $C_n = C_{50} + C_{51} + C_{53}$

$I_{drcp} = 2 * V_{ntc} / R_i$   
where  $R_i = R_{34}$   
Set  $R_i$  such that  $I_{drcp} = 38.8\mu A$  at full load

Nominal locset=60uA for OCP,  
Rocset=R22 is allowed to slightly fine tune OCP  
 $V_{drcp} = I_{drcp} * R_{21}$   
 $I_{mon} = 3 * I_{drcp}$

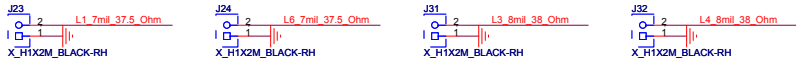
OCP 79A  
IMAX 60A





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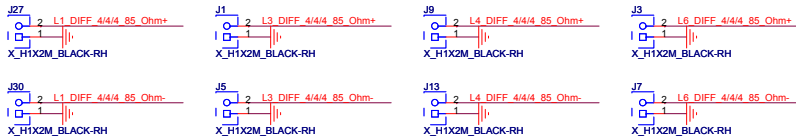
38 OHM



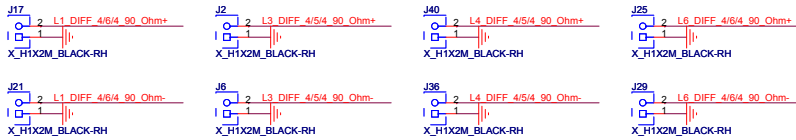
50 OHM



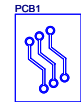
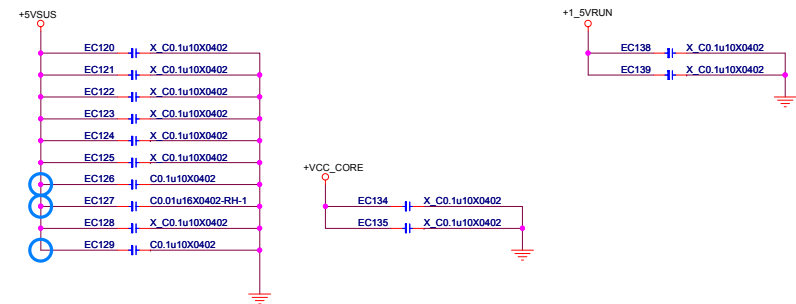
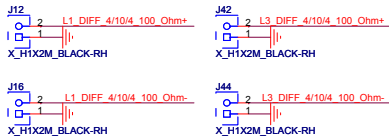
85 OHM



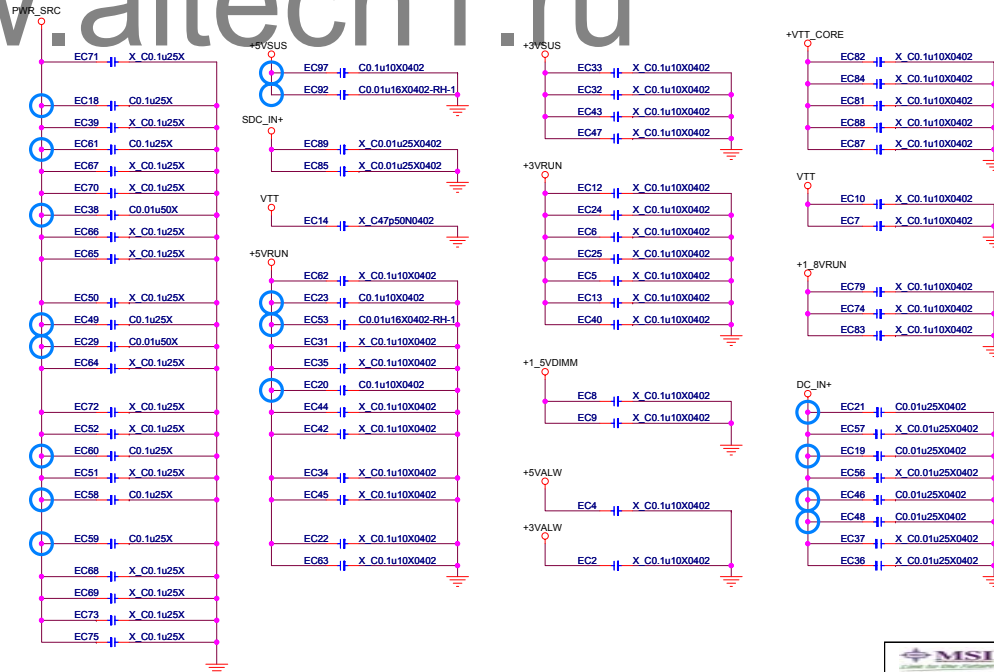
90 OHM



100 OHM

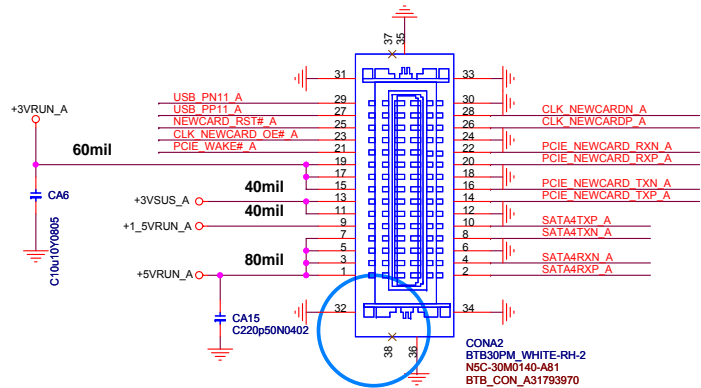


P30-16F1110-H73

BAT1  
BAT-BCR2032P-RHBIOS\_LABEL  
MP えHDMI\_LABEL  
ン

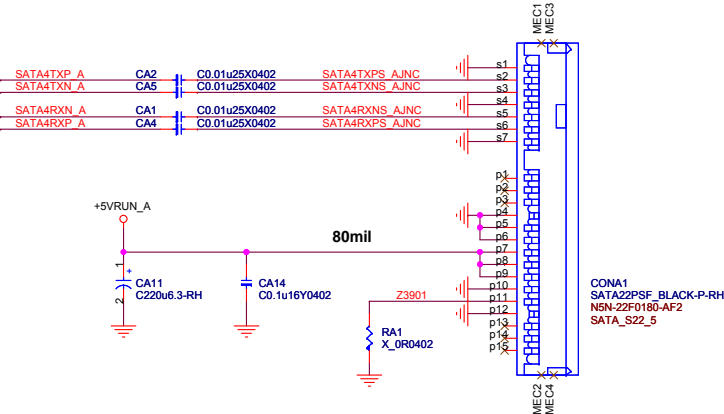


BTB Conn

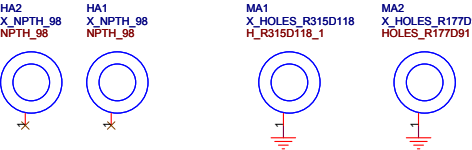
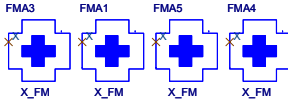
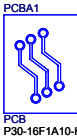
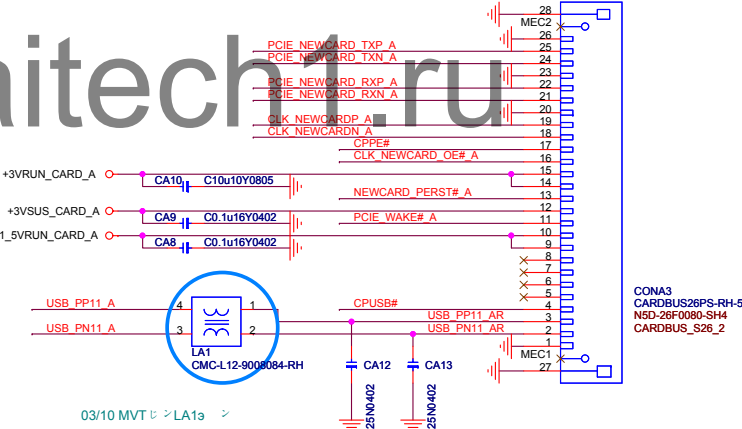
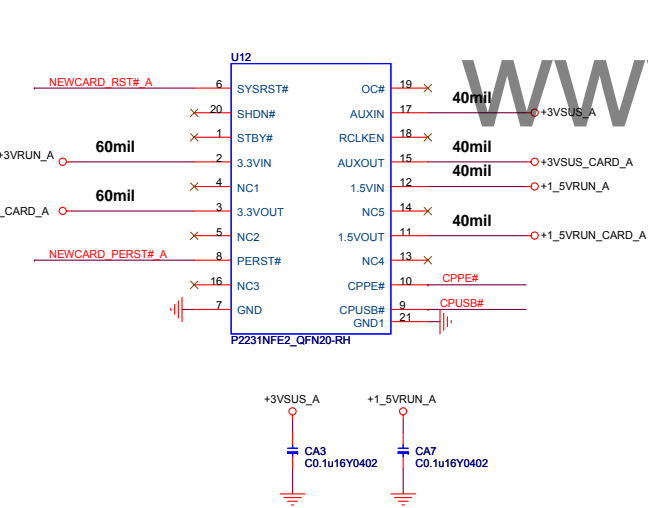


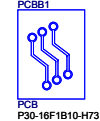
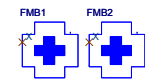
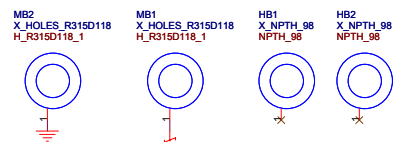
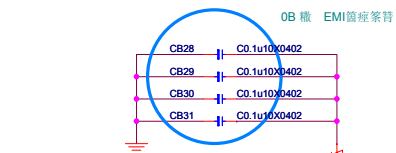
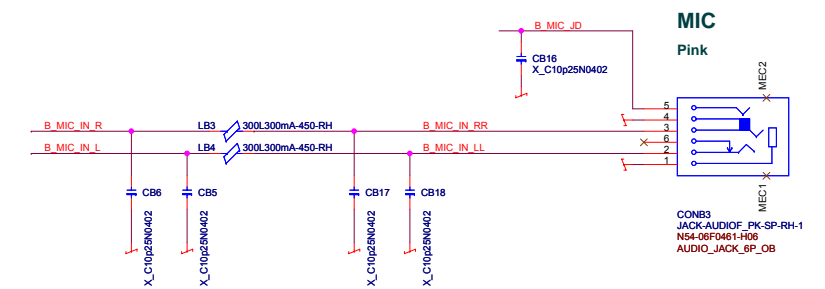
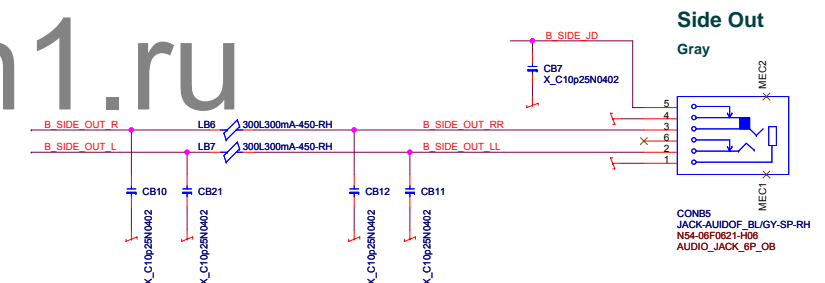
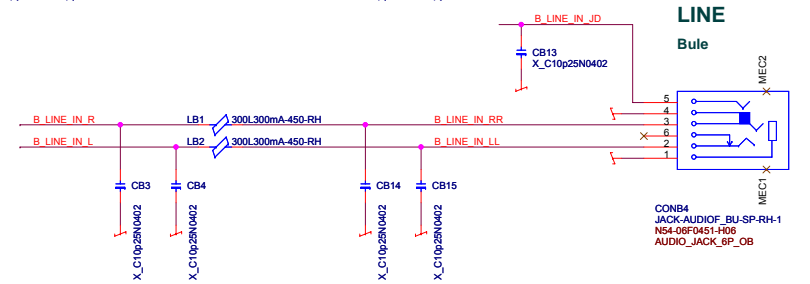
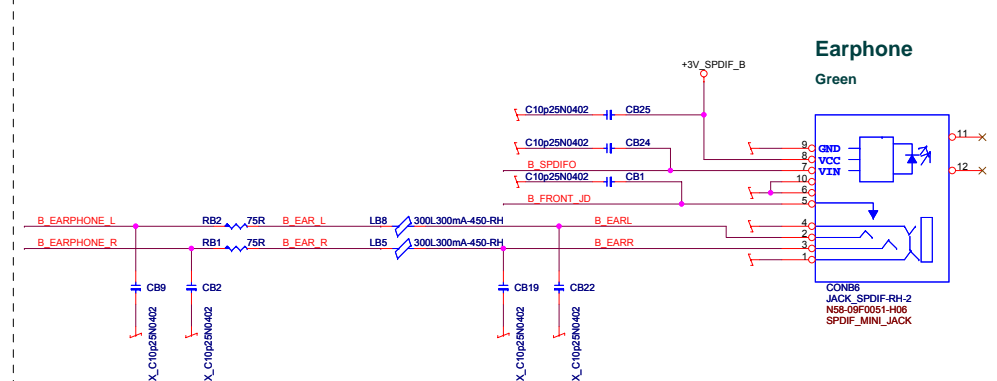
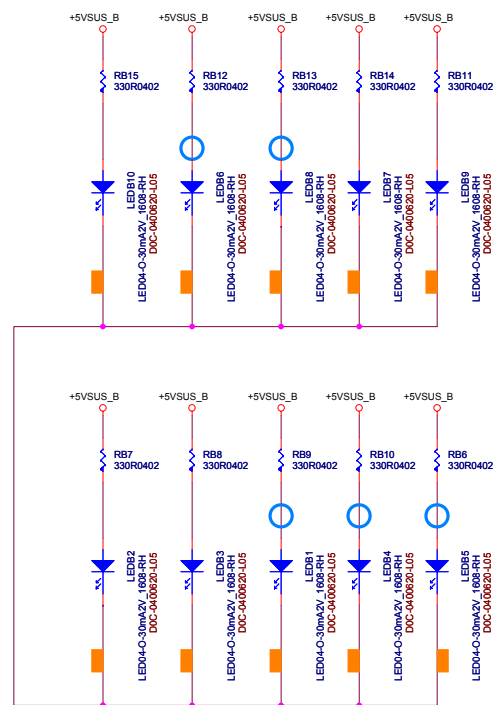
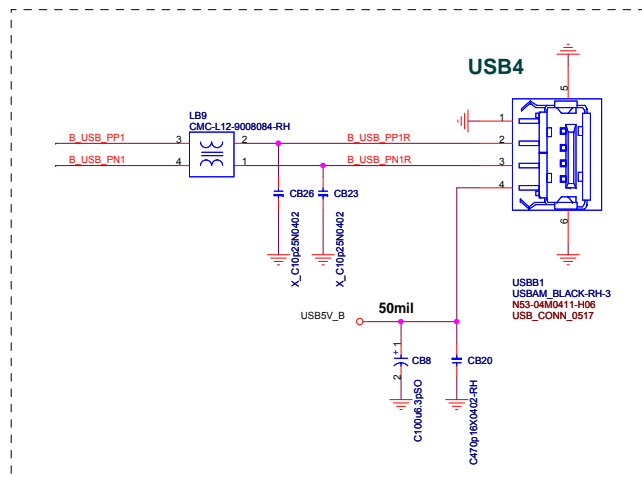
厂ノはFootpimt ( み 根じん) 数 新PIN は

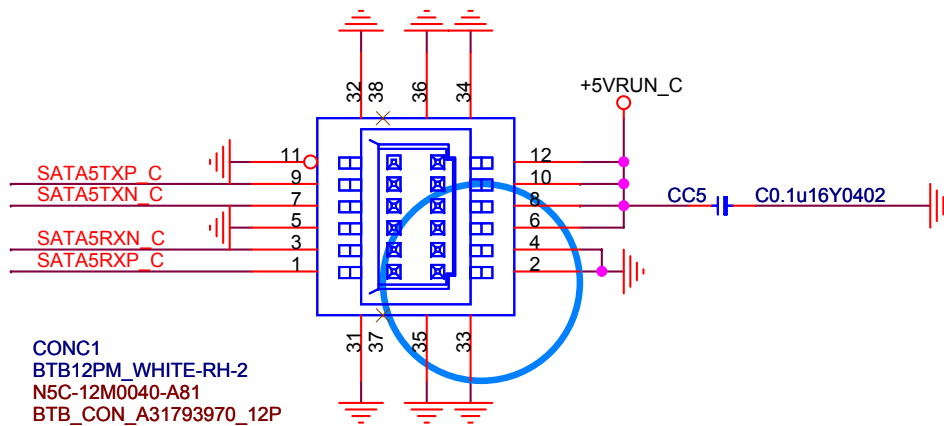
SATA HDD1



NewCard



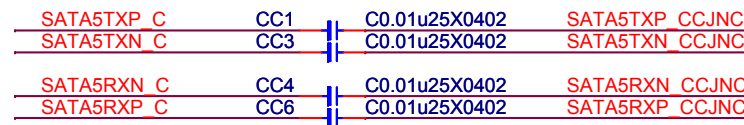




厂ノ はFootpimt ( み 糧じん)

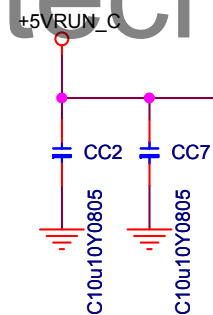
1/12 0B 3 腹

籤 狝 は

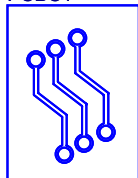


CONC2  
SATA22PSF\_BLACK-P-RH-3  
N5N-22F0210-A81  
SATA\_S22\_8

+5VRUN\_C

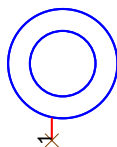


PCBC1

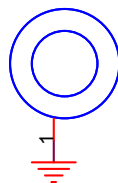


PCB  
P30-16F1C10-H73

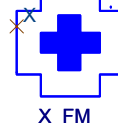
HC2  
X\_HOLES\_R177D91  
HOLES\_R177D91



HC1  
X\_HOLES\_R177D91  
HOLES\_R177D91

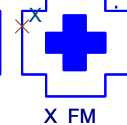


FMC1



X\_FM

FMC2



X\_FM



MICRO-STAR INT'L CO.,LTD.

Title

HDD2

Size  
A

Document Number

MS-16FC

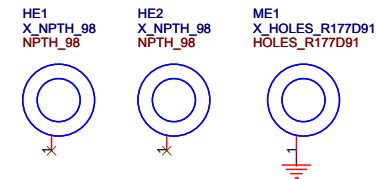
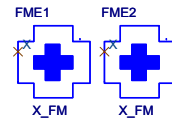
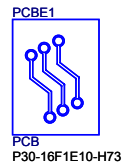
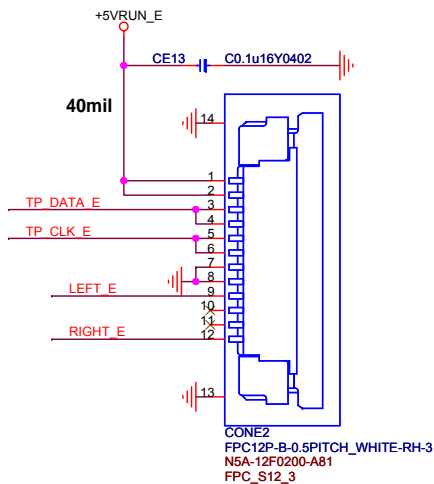
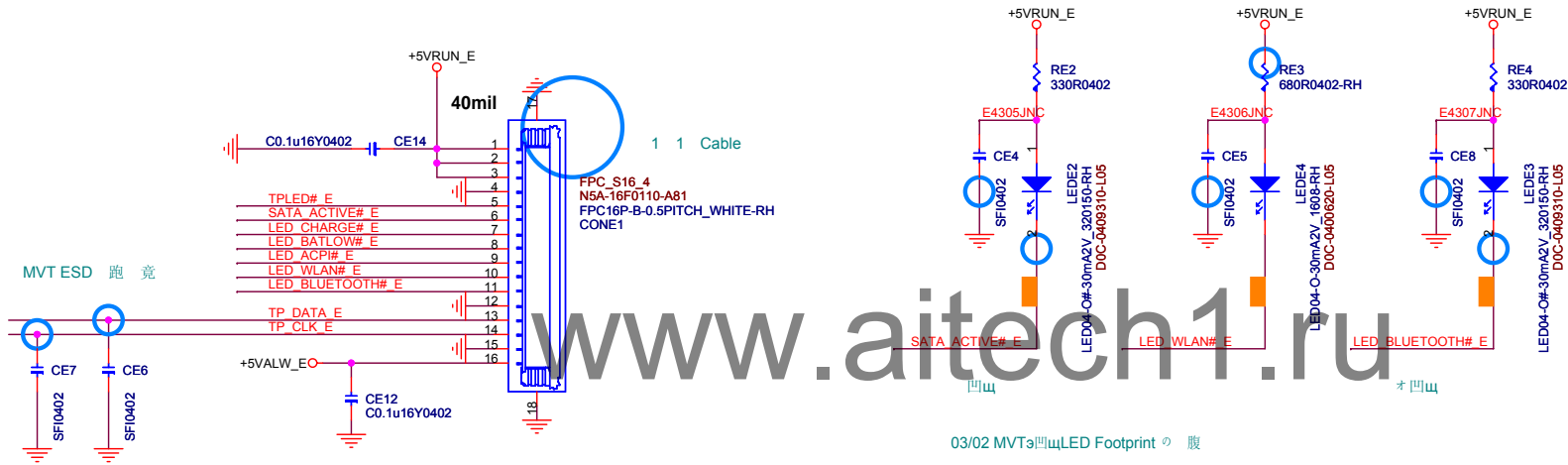
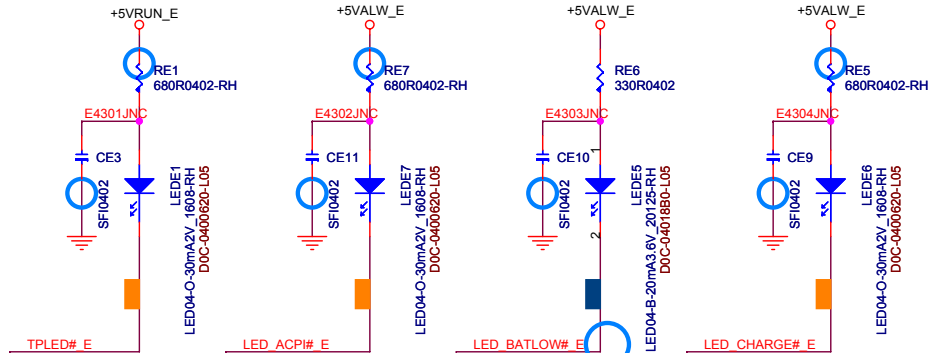
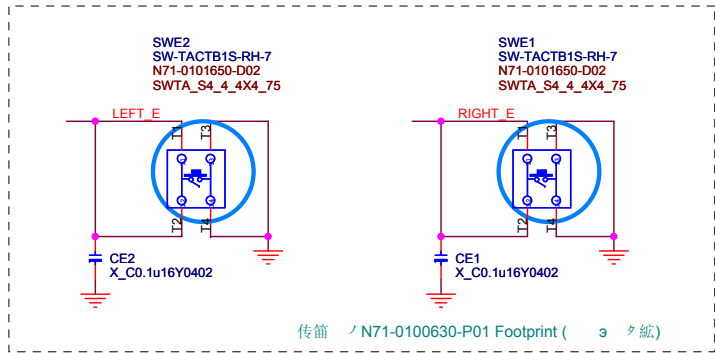
Rev  
1.1

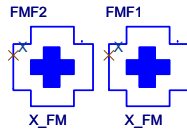
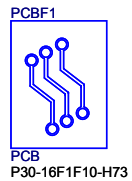
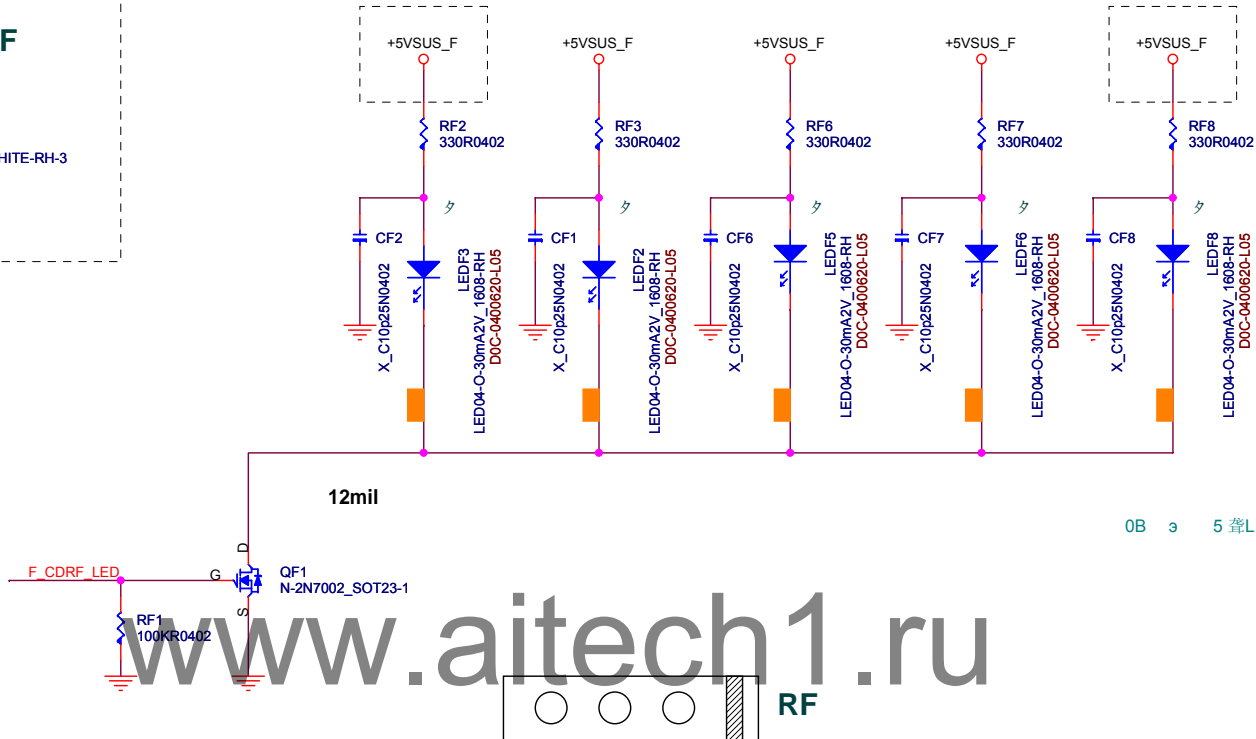
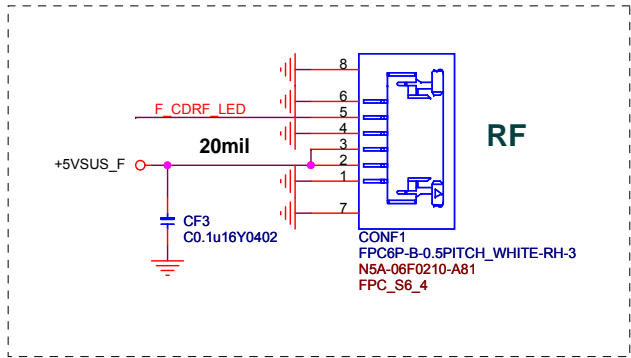
Date: Monday, March 29, 2010


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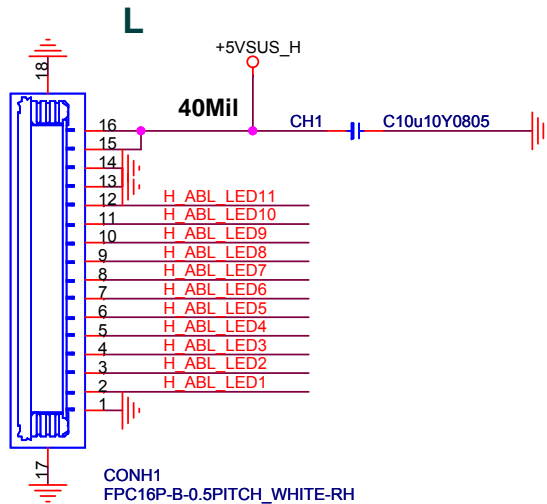




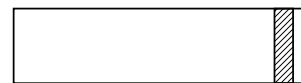
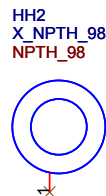
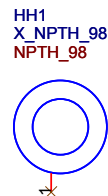
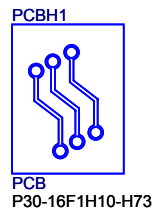
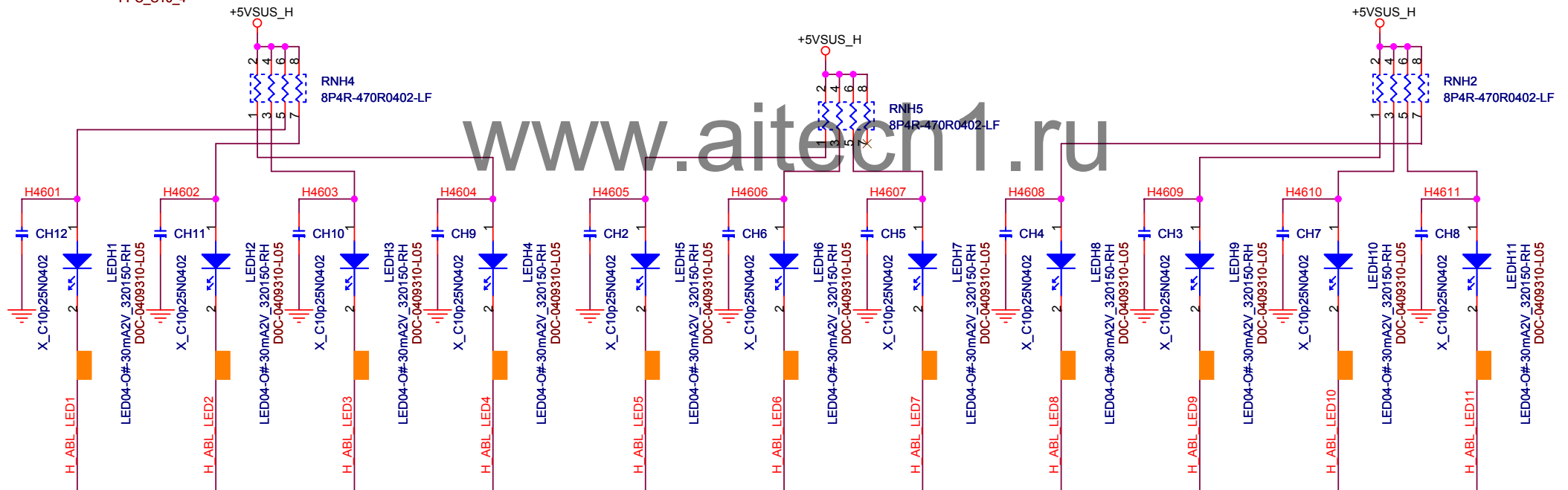


 <b>MICRO-STAR INT'L CO.,LTD.</b>		
Title <b>CDLED_RF</b>		
Size Custom	Document Number <b>MS-16F1F</b>	Rev 1.1
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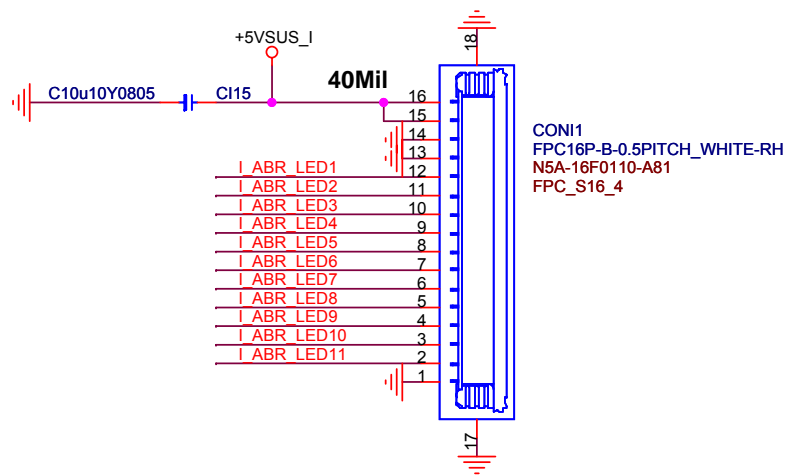


03/02 MVT LED Footprint の 腹

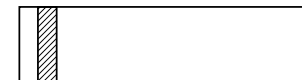


Title		
AB Size LED_L		
Size	Document Number	Rev
Custom	MS-16FH	1.1
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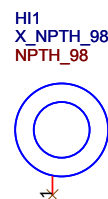
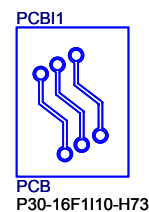
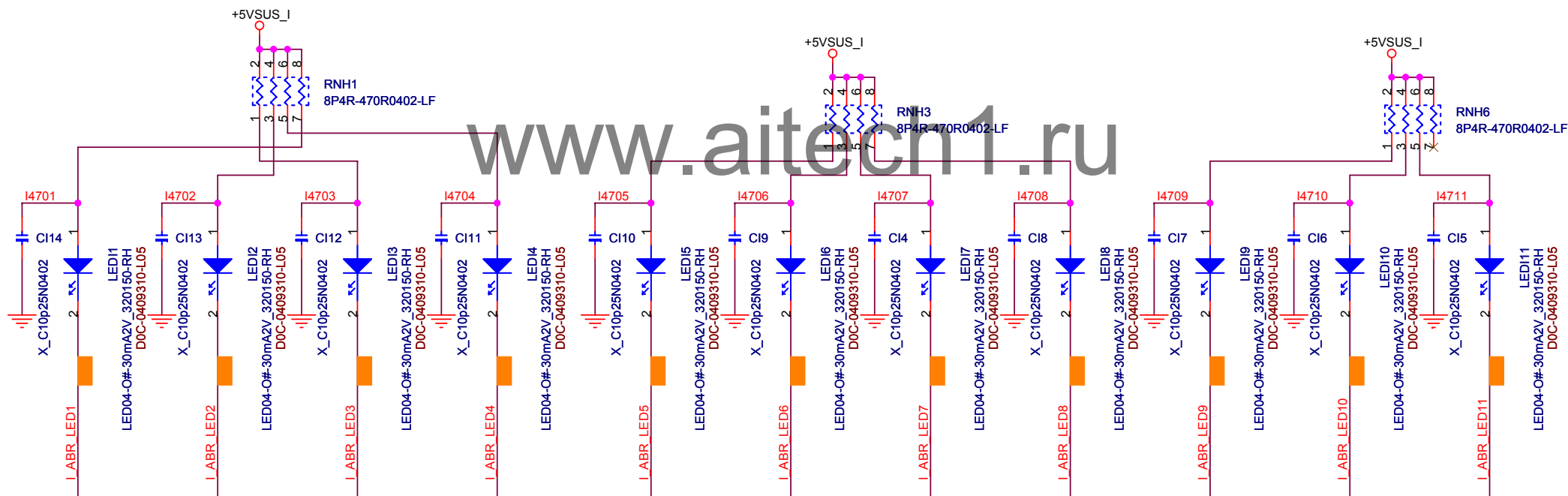




R

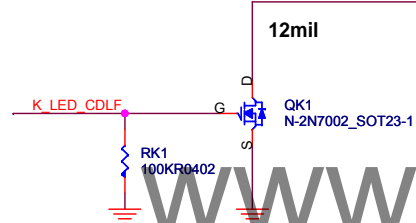


03/02 MVT LED Footprint の 腹

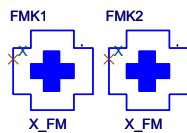


Title		
AB Size LED_R		
Size	Document Number	Rev
Custom	MS-16FI	1.1
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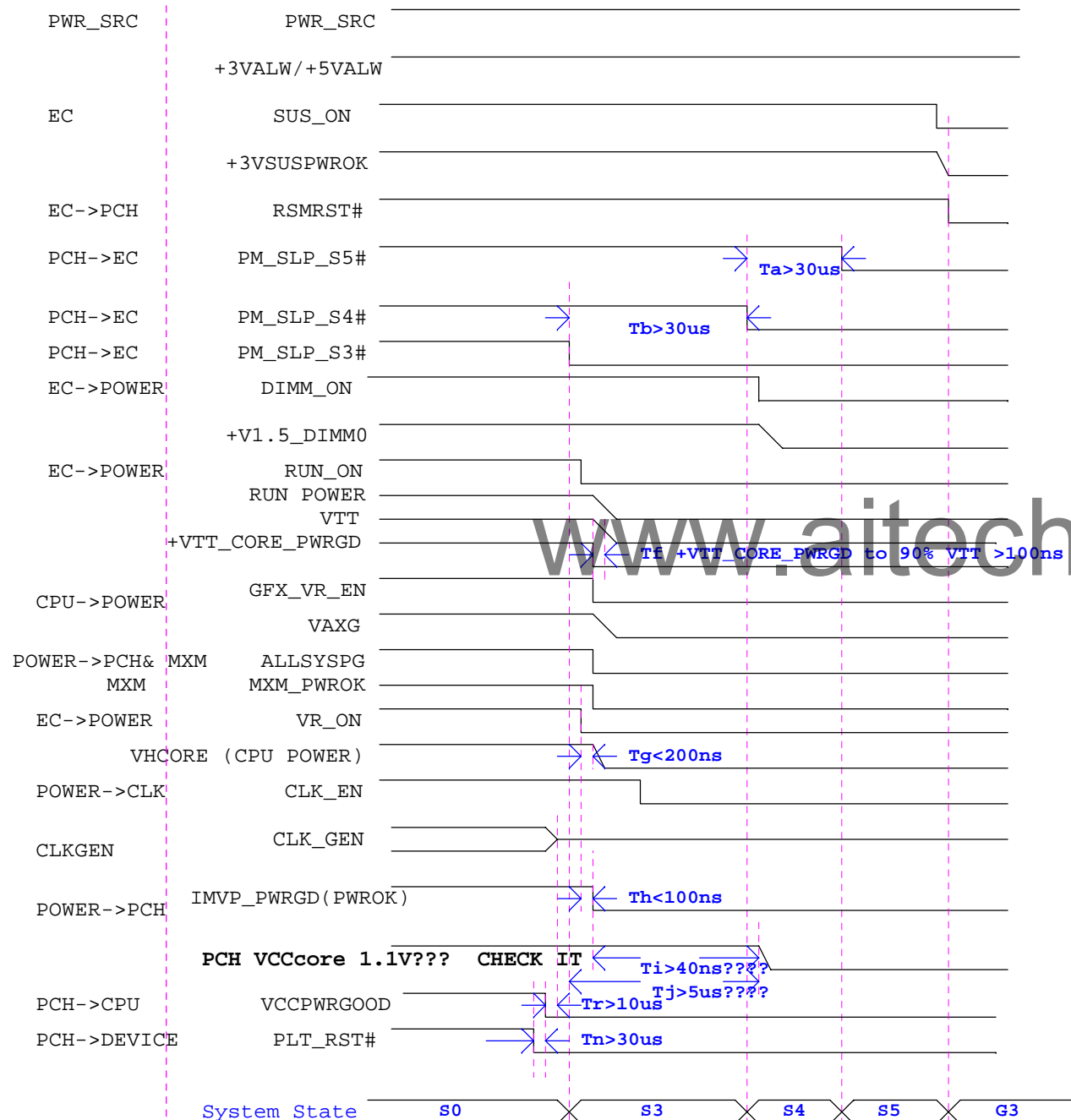


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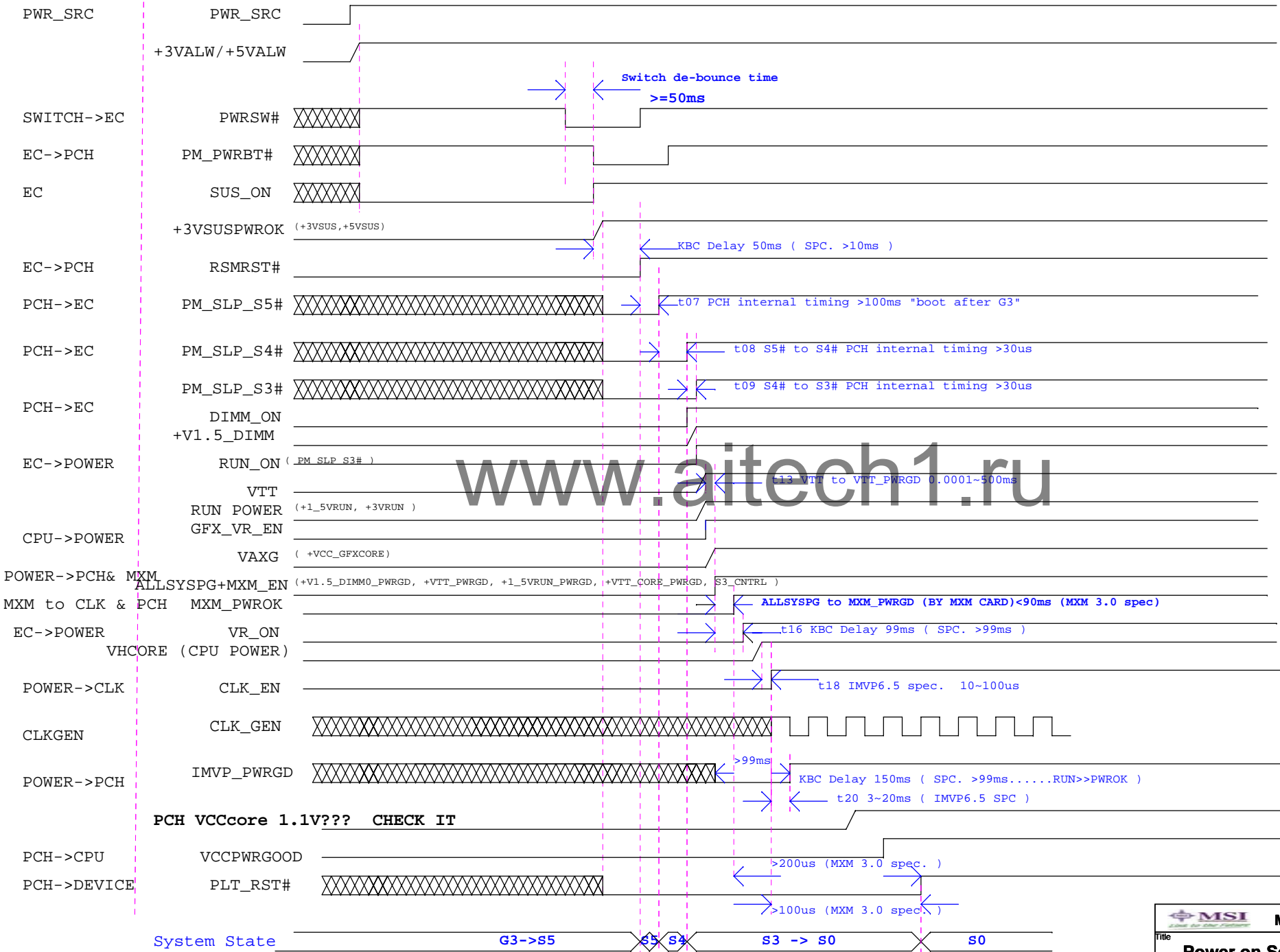


Title				
<b>CD Size LED_LF</b>				
Size	Document Number			Rev
Custom	<b>MS-16FK</b>			1.1
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# Power down Sequence DC mode S0 to G3



# Calpella System Power on Sequence DC mode



- 0A ㊟ 0B    タ兜へ
1. 12/23 0B    ㊟ RD15 24K 1% ㊟19K 1% (16F1D)
2. 12/23 0B    ㊟ U26.U9 PIN5/PIN2 が粘
3. 12/23 0B    ㊟ CN1 (Keyboard Conn) PIN は 锣
4. 12/23 0B    ㊟ CPU VID 筈 非    VTT (Page 36)
5. 12/23 0B    ㊟ PCH    腹0B01-BD82H85-I06
6. 12/23 0B    ㊟ PC84.PC112 传    (6.3V環溃)
7. 12/23 0B    ㊟ PC96 传    ㊟ X7R
8. 12/23 0B    ㊟ PC87.PC88 传
9. 12/24 0B    ㊟ R132.R134.R131.R135 ㊟10K 1% ㊟1K 1% (For 4DIMM Driving)
10. 12/24 0B    ㊟ 撒    レン R317.R318.R319.R320
11. 12/25 0B    ㊟ 撒    A1 DDR3 DIMM Slot
12. 12/28 0B    ㊟ C127.C137.C149 ㊟0805 ㊟0603 10uF
13. 12/30 0B ㊟CON5 ㊟4Pin ㊟ 5Pin    169x Digital MIC ノ
14. 12/30 0B    ㊟R66.R67.R182 ㊟0 稼〃㊟Copper
15. 12/30 0B    ㊟PCH    场25MHz( い    ン R89.C89.X1.C92)(    ン R94)
16. 01/04 0B    ㊟U8 SMBUS    罅
17. 01/04 0B    ㊟R9 ㊟100K㊟10K
18. 01/04 0B 撒    PEC11 22UF筈背筒疵
19. 01/06 0B 撒    SPDIFO2腐腹    MXM Slot
20. 01/06 0B 撒    EPF021\_OPMODE/EPF021\_RST ㊟EC    北
21. 01/06 0B    ㊟U15 CardReader    腹    A3    セ
22. 01/06 0B    ㊟PU2.PU8 ノ    ㊟I34-0626319-U33 侶    EOL
23. 01/11 0B    ㊟R249.R283.R281.R285 ㊟0 稼〃㊟Copper
24. 01/11 0B 撒    R342.R343.R344 0 稼〃 (Audio)
25. 01/11 0B    ㊟U7 BIOS    奔Socket
26. 01/11 0B    ㊟PR144    ン
27. 01/11 0B    ㊟PR161    (System Power)
28. 01/11 0B    ㊟PR65.PR102    (CPU Power)
29. 01/11 0B 撒    PAD7 紆    ン
30. 01/12 0B    埃FME3.FME4    厥腿
31. 01/12 0B    ㊟MS16F1J 5葎LED跑    葎SIZE
32. 01/12 0B    ㊟CONC1 策ンノ
33. 01/13 0B    ㊟RNJ1 Swap Pin
34. 01/13 0B    ㊟PU2 俱舱膾溃IC い    ン (VTT筈溃)
35. 01/13 0B 撒    PQ4俱舱と溃IC (1.5VDIMM筈溃)

- 0B ㊟ MVT    タ兜へ
01. 02/03 撒    NewCard 臓ンの脸搦
02. 02/11 ㊟RD15    15.8K 1%
03. 02/11    埃G8. G9 Copper (+VTT\_CORE)
04. 02/11    埃G5. G6 Copper (+1\_5VDIMM)
05. 02/11    埃G7 Copper (+0\_75VRUN)
06. 02/11    埃G1.G3 Copper (+1\_8VRUN / VTT)
07. 02/11    埃G2.G4 Copper (+3VSUS / +5VSUS)
08. 02/12 ㊟PR108 Copper
09. 02/25    R333 0 稼〃㊟Copper
10. 02/25    R195 0 稼〃㊟Copper
11. 03/01    埃R192    钼硃硃
12. 03/01    ㊟R102 ㊟Copper
13. 03/01    ㊟R176 ㊟Copper
14. 03/01    ㊟PR79.PR75 ㊟Copper ㊟10K (CPU PWM)
15. 03/01    ㊟PR71.PR76 ㊟Copper ㊟8.2K (CPU PWM)
16. 03/01    ㊟PR78.PR69 ㊟Copper ㊟12K (CPU PWM)
17. 03/01    ㊟R181 ㊟Copper
18. 03/01    ㊟R45.R46 ㊟Copper
19. 03/04    ㊟R226.R227.R124 ㊟0稼〃㊟Copper
20. 03/04 ㊟CON13 い    ン (BIOS Debug Port)
21. 03/04    ㊟R94 ㊟0稼〃㊟Copper
22. 03/04    ㊟R53.R260.C370 い    ン (PC Beep)
23. 03/04 零件SATA HDD1.HDD2 瘰瘰
24. 03/10 撒    U28半レイ For 3D Panel
25. 03/10    ㊟レン PEC35 い    ン
26. 03/10    ㊟レン LA1.LI9 ㊟    ン (EMI ㊟)
27. 03/10    ㊟R308.R309.R335.R336 ㊟0 稼〃㊟Copper
28. 03/11    ㊟R28.R29 ㊟0 稼〃㊟Copper

- MVT ㊟ 1.1    タ兜へ
01. 凹ㄣLED Footprint ㊟LEDS\_12\_21\_B\_C\_T ㊟ LEDS\_12\_21\_B\_C\_T\_T